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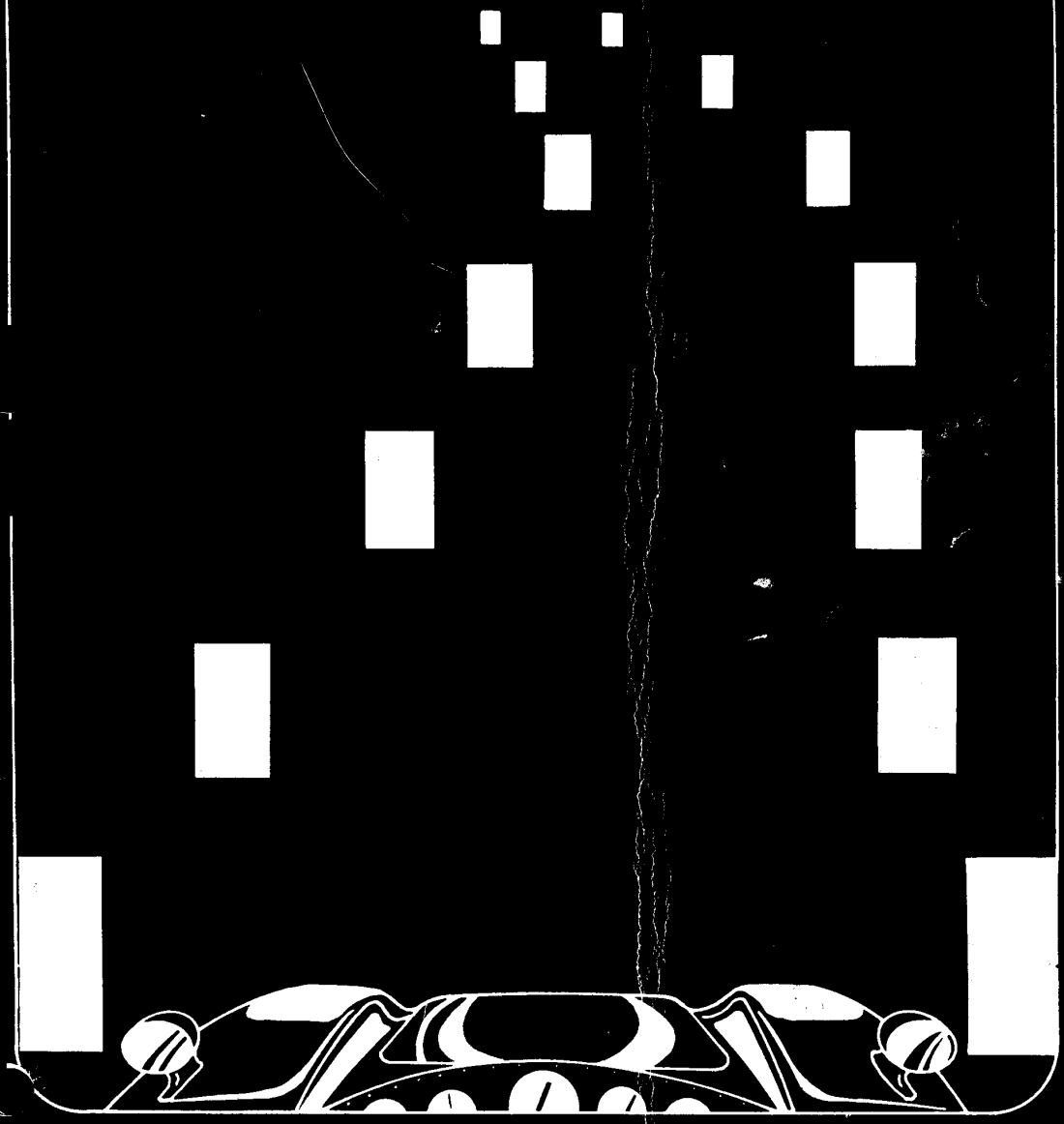
NIGHT DRIVER™

Operation, Maintenance and Service Manual

ATARI™



NIGHT DRIVER

Operation, Maintenance and Service Manual

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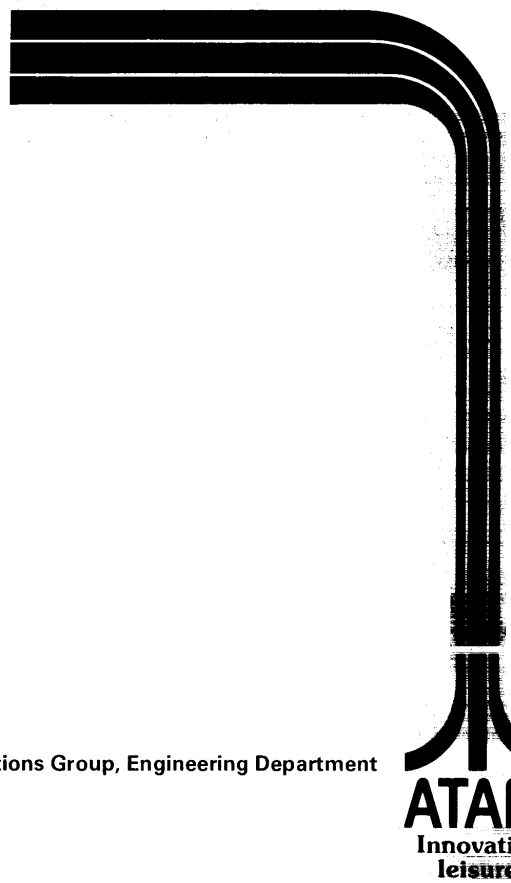

By the Publications Group, Engineering Department

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I. INTRODUCTION

1.1 PHYSICAL DESCRIPTION OF GAME

Atari's Night Driver is a one-player driving game. The game is packaged in its own distinctively styled upright cabinet that rests directly on the floor. A 23-inch TV monitor is mounted in the top front of the cabinet, with the monitor viewing screen slightly tilted back from vertical. (Figures 7-1 and 7-2 in Section VII and drawing number A006264-01, in Section IX of this manual, provide external and sectional views of the game cabinet.) The TV monitor is covered with a Plexiglas panel.

Player-operated controls are mounted directly below the TV monitor viewing screen on the front of the game cabinet. The controls consist of a steering wheel, a four-speed gear shifter, an accelerator foot pedal, a three-position rocker switch, and a pushbutton. The rocker switch is labeled NOVICE TRACK, PRO TRACK, and EXPERT TRACK. The pushbutton switch is labeled START. Two speakers mounted at the front of the game cabinet provide game sound.

Two identical coin mechanisms are mounted on the lower front center of the game cabinet, below the steering and shifting controls. Either of these two mechanisms can initiate play. The cash box is located behind a locked access door to the coin mechanisms.

1.2 SUMMARY OF GAME PLAY

The player's objective is to keep the car within the pylon boundaries of the track and to go as fast as possible.

After the proper coins have been inserted in the coin mechanism, the choice of which track to be played should be made. The difficulty factor of the tracks is determined by the track select rocker switch. In other words, the PRO TRACK is more difficult than the NOVICE TRACK, and the EXPERT TRACK is more difficult than the PRO TRACK.

Once the determination of the desired track is made, a player must press the start pushbutton. This begins the game play and the game time begins counting down from 100.

Now with the left hand on the steering wheel, the right hand on the four-speed gear shifter, the right foot on the accelerator foot pedal, and the sound of an idling motor, the player may begin to "drive" the car along the racetrack.

Acceleration is as in a real car. Start out in anything but first gear and the car accelerates slowly. Start out in first gear and the car accelerates nicely. Once the car is moving, shifting into progressively higher gears increases the speed of the car. If the car goes into a turn too rapidly, there will be the sound of the car skidding from the game cabinet speakers. If the car "drives" into a track boundary, a crash sound will be heard from the game cabinet speaker and the TV monitor viewing screen will flash.

The outstanding feature of Night Driver is that it is a game of skill. The player must skillfully manipulate his car along the track in a race against time.

II. SPECIFICATIONS

2.1 GENERAL

Cabinet Dimensions:	Height 73 inches, Width 25¼ inches, Depth 32 inches.
TV Monitor:	Black and white 23-inch screen, video input.
Coin Mechanisms:	Two identical mechanisms, accept only quarters.
Cash Box:	Removable; located behind locked access door to coin mechanisms.
Power Cord:	Approximately 6 feet long, extends from rear of game cabinet and has grounded three-prong plug for conventional grounded wall outlets.
On/Off Switch:	Hidden above the Accelerator Foot Pedal for owner/operator access.
Self-Test Switch:	Located at the inside front of game cabinet to the immediate left of coin box.
Lighting:	One 18-inch fluorescent tube for cabinet lighting. One 9-inch black light for bezel lighting.

2.2 ELECTRICAL

Power Requirements:	Uses conventional grounded wall outlet providing 110 volts AC, 60 Hz, single phase, rated at about 200 watts.
Fusing:	All fuses accessible from Rear Access Door of the game cabinet; TV monitor has two 3AG 1-amp slow blow, 250 volt fuses and remainder of game is protected by two 3AG 3-amp quick blow, 250 volt fuses, both mounted side-by-side on the Electronics Tray Assembly.
Power Interrupt Switches:	These are safety interlock switches located inside the game cabinet Rear Access Door. They cause the removal of AC power to the game when the access door is opened.

2.3 ENVIRONMENTAL

Operating and Storage Temperature Range:	From 32 degrees Fahrenheit to 120 degrees Fahrenheit (ambient temperature).
Relative Humidity:	Maximum of 80% without condensation.

2.4 OWNER/OPERATOR OPTIONS FOR STRUCTURING OF GAME PLAY

Cost:	• 25¢ per player • 25¢ per two players • 50¢ per player
Game Length:	• 50 seconds • 75 seconds • 100 seconds • 125 seconds
Extended Play:	See paragraph 3.4.2 in Section III.

2.5 ACCESSORIES AVAILABLE ON SEPARATE ORDER

Video Probe:	Order from Atari
Computer Test Fixture:	Order from Atari, catalog no. CTF-1
Computer Test Fixture Night Driver Adaptor:	Order from Atari, Program Plugs and Test PROMs

III. DESCRIPTION

3.1 FUNCTIONAL DESCRIPTION OF GAME

The block diagram in Figure 3-1 illustrates the major functional parts of the Night Driver Game. Note that the game printed circuit board (hereafter referred to as PCB) sends composite video signal to the TV monitor and a separate audio signal to the game cabinet speaker.

3.2 GENERAL INFORMATION

General information about the game in the following subparagraphs provides a background for the Installation Instructions in Section V of this manual, and the description of Game Sequence in paragraph 3.3 of this section.

3.2.1 Energizing the Game:

The game is energized by inserting the AC power plug into an active wall outlet that provides the specified AC power as listed in Section II, Specifications, of this manual. The Power On/Off switch, hidden above the accelerator foot pedal must be set to the "on" position.

3.2.2 TV Monitor:

The game's TV monitor is a self-contained transistorized television monitor with composite video input. Because the composite video signal sent to the monitor by the control circuitry differs in many respects from the signal derived from commercial TV broadcasts, the picture appearing on the screen is unlike that of a home TV set and the monitor does not produce any sound.

3.2.3 TV Monitor Picture:

The game's TV monitor picture produces only two levels of video (white and black), instead of more or less continuous shades of gray seen on a home TV screen.

3.3 GAME SEQUENCE

3.3.1 Operating Modes:

During normal use, Night Driver can be described as operating in one of two modes—attract and play. Connecting the power cord to the proper AC source energizes the game and the game will be in the attract mode. The game remains in the attract mode until the proper number of coins have been inserted and the coins clear the coin mechanism and the start pushbutton has been pressed. Pressing the start pushbutton initiates game play and the game timer begins counting down from 100 by one-digit increments. When the timer reaches zero, the game goes into the attract mode (see Owner/Operator Options, paragraph 3.4 of this section).

3.3.2 Attract Mode:

Figure 3-2 illustrates the TV monitor display during the attract mode. During the attract mode the

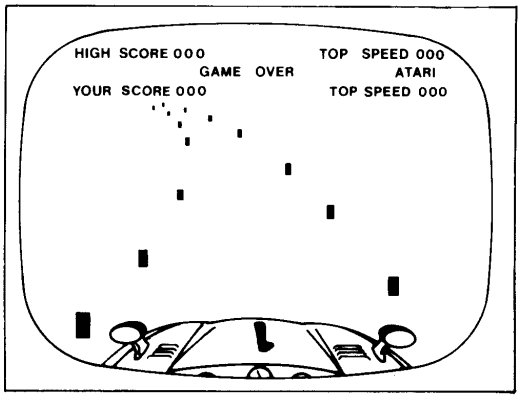


Figure 3-2 Attract Mode TV Monitor Display

TV monitor will display the highest score and speed obtained by a player since the last power-up of the game. The words "GAME OVER" will flash on and off. The roadway pylons will move as if the car is moving along the road.

3.3.3 Play Mode:

Figure 3-3 illustrates the TV monitor display during the play mode. During this mode the TV monitor will display a roadway that advances when the accelerator foot pedal is stepped on. Shifting the gear shifter through the gears increases the advancing speed of the roadway pylons. If the car comes into contact with one of the pylons, the roadway pylons will stop advancing, the TV monitor display will flash, and a crash sound will come from the game speakers. If the car "drives" off the roadway, the following message will be displayed on the TV monitor:

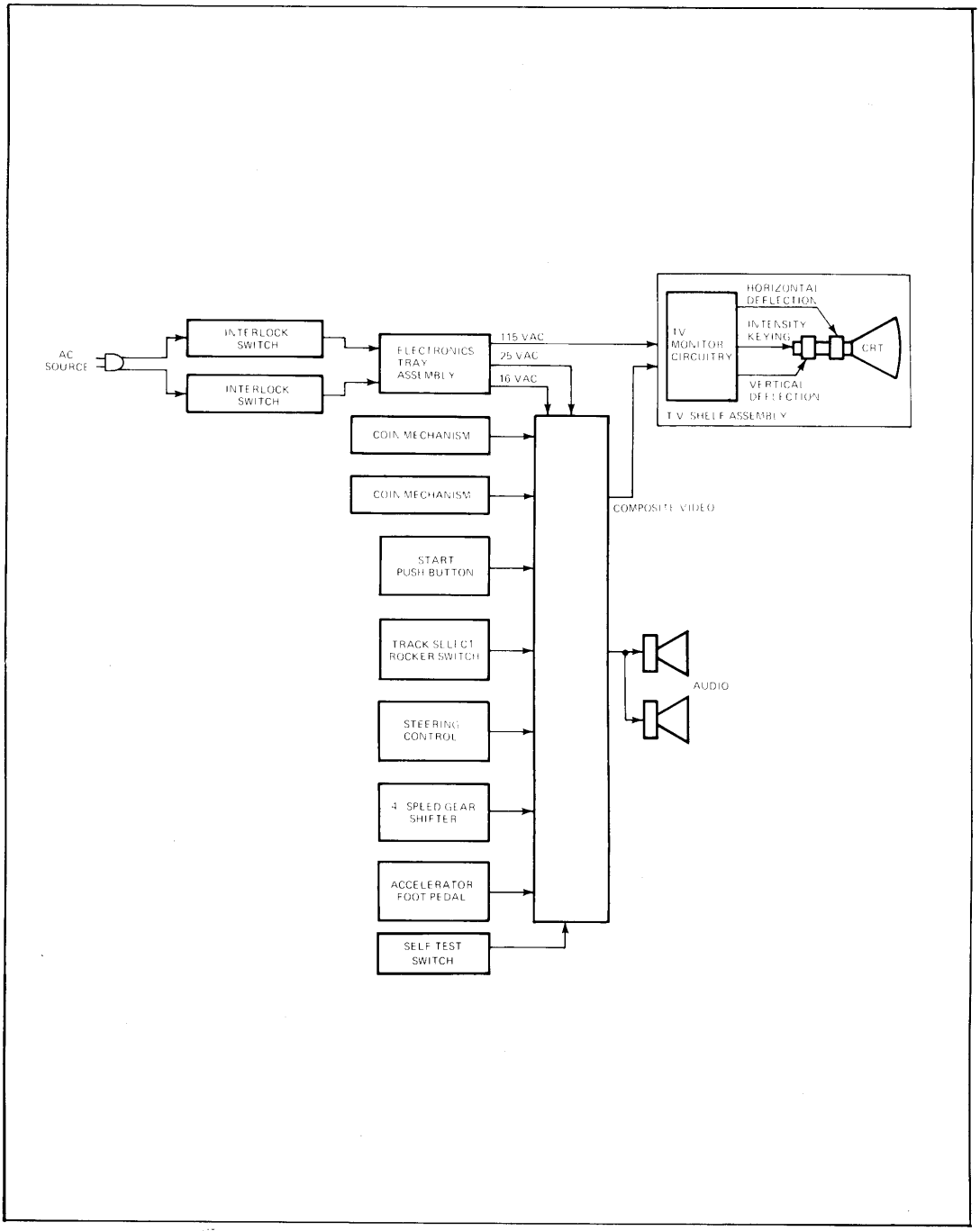


Figure 3-1 Functional Block Diagram of Night Driver Game

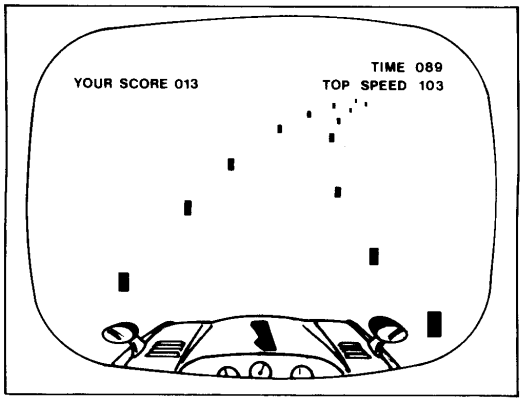


Figure 3-3 Play Mode TV Monitor Display

OFF THE ROAD
WAIT FOR THE TOW TRUCK

After approximately three seconds, the message will disappear and the roadway pylons will reset so that the car is again between the roadway pylons.

Table 3-1 Price/Time Per Game Options Settings

SWITCH POSITION	SECONDS	PLAY PRICE
0	50	2 plays/coin
1	50	1 play/coin
2	50	1 play/coin
3	50	1 play/2 coins
4	75	2 plays/coin
5	75	1 play/coin
6	75	1 play/coin
7	75	1 play/2 coins
8	100	2 plays/coin
9	100	1 play/coin
A	100	1 play/coin
B	100	1 play/2 coins
C	125	2 plays/coin
D	125	1 play/coin
E	125	1 play/coin
F	125	1 play/2 coins

3.4 OWNER/OPERATOR OPTIONS

3.4.1 Price/Time Per Game Options:

Mounted on the Night Driver PCB is a hexadecimal switch that has fifteen different switch positions. This switch, located at coordinates L10 on the PCB (see Figure 3-4), may be adjusted for the desired price/time structuring as indicated in Table 3-1. The Switch Position column indicates the alphanumeric that is printed on the switch itself, as well as the first character immediately following the word OPTIONS in the TV monitor display during self-test (see Figure 5-1). The Seconds column indicates the total play length (not including bonus, as adjusted according to paragraph 3.3.2). The Play Price column indicates the Price to play the game.

3.4.2 Bonus/Track Difficulty Options:

Mounted on the Night Driver PCB is a four toggle DIP(dual in-line package) switch. This switch (see Figure 3-4), located at coordinates M10 on the PCB, may be adjusted for no bonus time, bonus time, or "hard-to-get" bonus time. Also this switch may be adjusted to change the tracks, thus decreasing the "player familiarity" factor. These options are all listed in Table 3-2. The Switch Position column indicates the toggle position of switch M10 on the Night Driver PCB. The Self-Test Display column indicates the four characters grouped together after the word OPTIONS in the TV monitor display during self-test (see Figure 5-1). The Option column indicates the option provided when that switch is in the ON position.

3.4.3 Volume Control:

Control for the volume of all game audio is located on the Night Driver PCB. This is a small potentiometer (R111) located on the component side of the PCB, as illustrated in Figure 3-4.

Table 3-2 Bonus Time/Track Familiarity Options Settings

SWITCH POSITION				SELF-TEST DISPLAY	OPTION
1	2	3	4		
OFF	OFF	OFF	OFF	0000	No option selected.
ON	OFF	OFF	OFF	1000	Toggle 1 provides bonus time (equal to game time) awarded for score of 350.
ON	OFF	OFF	ON	1001	Toggle 4 ON when Toggle 1 is ON makes bonus time score of 350 more difficult to achieve.
ON	ON	OFF	ON	1101	Toggle 2 reverses the turns of all three tracks.
ON	ON	ON	ON	1111	Toggle 3 has no function and is not connected in the circuit.

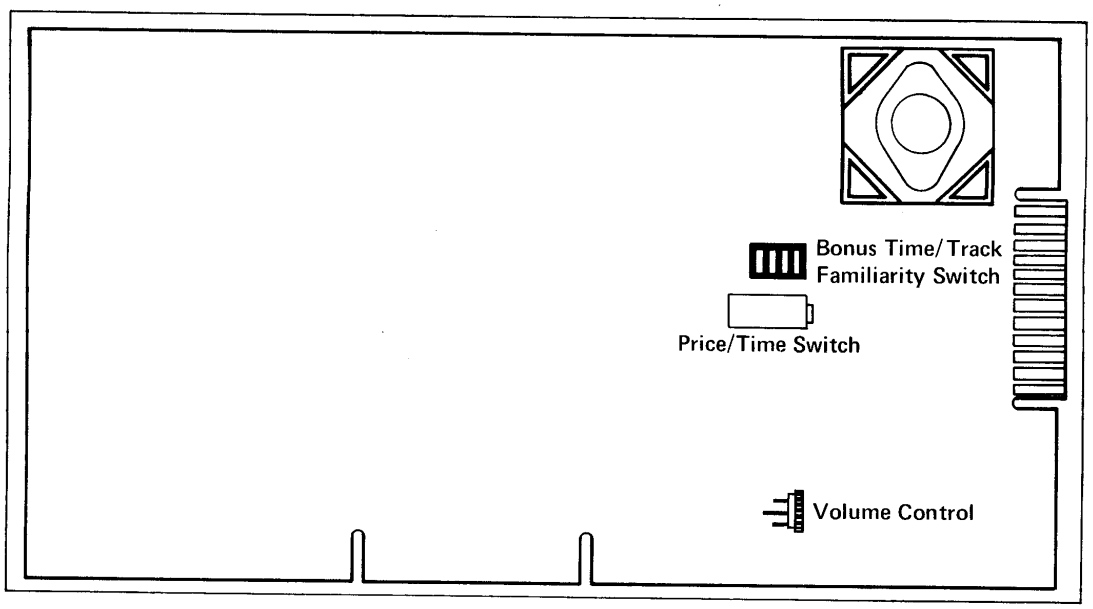


Figure 3-4 Locations of Owner/Operator Option Switches and Volume Control

IV. THEORY OF OPERATION

4.1 GENERAL COMMENTS

This section provides a technical description of the Night Driver PCB that is supplemental to the signal description in Section VIII, Troubleshooting. Section IX contains schematic diagrams, assembly drawings, and parts lists referred to in the following sub-paragraphs of this section. Figure 4-1 is a block diagram of the Night Driver PCB.

On the Night Driver PCB schematic diagram, drawing number 006231, the symbol P (appearing at various inputs of the integrated circuits) indicates a connection to +5 VDC through one of the 1K ohm resistors R7, R48, R52, R112.

For easy reference, the Night Driver PCB is divided into 126 sections. These sections are identified by letters A through R (skipping letters G, I, O, and Q, because they may easily be confused with numbers 6, 1, and 0) for the short side of the PCB and numbers 1 through 9 for the long side of the PCB. For example, sheet 3 of schematic 006321 illustrates a random-access memory (RAM) H6 at the upper left of the drawing. The component hardware of RAM H6 will be found at coordinates H and 6 on the PCB.

4.2 COMPONENTS OF THE MICROCOMPUTER SYSTEM

The microcomputer system carries out complex tasks of the game by performing a large number of simple tasks. Control of the system is the primary function of the Microprocessor. The Microprocessor causes the system to perform the desired operations by addressing the Program PROMs (programmable read-only memories) for an instruction, reading that instruction, then executing the simple task dictated by that instruction. Temporary storage of data necessary for the execution of a future instruction, such as arithmetic operation, takes place in the Page Zero memory.

4.2.1 Program PROMs (bottom of schematic sheet 3):

The Program PROMs consist of read-only memories (ROMs), permanently programmed by Atari to execute the Night Driver game. This memory has the capability of outputting eight bits of data for each of 2,048 combinations of ones and zeros on the ten address inputs. In computer terminology, this is stated as a memory size of 2K x 8.

The Night Driver game contains one of two combinations of ROM chips to make up the Program PROMs, depending on when the individual Night Driver PCB was manufactured. For the early production models, Program PROMs consist of eight chips (as illustrated to the left of the word PROGRAM PROMS on the schematic diagram). Later production models consist of two chips (as illustrated to the right of the word PROGRAM PROMS on the schematic diagram). The eight Program PROM chips are completely interchangeable with the two Program PROM chips, but need not be retrofit.

Since data in the Program PROMs is a permanent physical configuration of the PROM chips, the data is not lost when power is disconnected from the game or when the chip is removed from its socket. Since the Program PROMs consist of read-only memories, the result of an address input can only be the "reading" of data stored in the manufacturing process. It is not possible to "write" in more data. (The term PROM stands for programmable read-only memory. To Atari, this means that the chip is a programmable ROM. To you, this chip is only a ROM.)

4.2.2 Page Zero Memory (right side of schematic sheet 3):

Page Zero memory consists of two random-access memories (RAMs). Data may be stored in Page Zero memory (called "writing" Page Zero), then later recalled (called "reading" Page Zero). Memory size of Page Zero is 512 x 8.

In order to read Page Zero, R/W (pins 16) input of the chips must be a high logic level and OD (pins 9) input must be a low logic level. To write Page Zero, R/W input must be a low logic level and OD input must be a high logic level.

As previously mentioned, data stored in Page Zero memory is for the purpose of performing operations on data as instructed by the Program

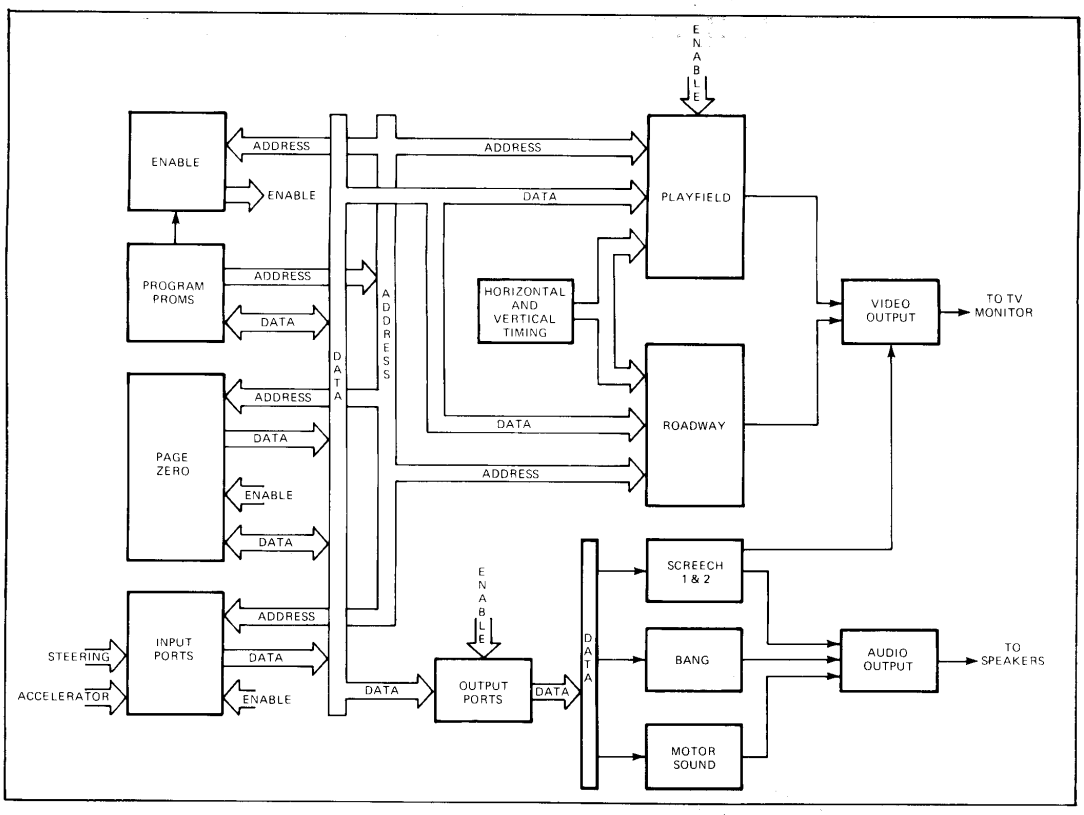


Figure 4-1 Block Diagram of the Night Driver PCB

PROMs. Since Page Zero is a temporary storage area, removing power from the chips will "erase" all stored data.

4.2.3 Microprocessor (left top of schematic sheet 2):

As mentioned earlier, the controller of the Microcomputer is the Microprocessor. From the Microprocessor, a sixteen-bit address bus addresses the Program PROMs, Page Zero, and Enable. An eight-bit bi-directional data bus serves as a path for transferring data from the Program PROMs, to and from Page Zero, and to the Roadway RAMs.

4.2.4 Tri-State Devices:

Tri-state devices, such as M1 of schematic sheet 2, are capable of having normal logic output of ones and zeros when disable (pin 1) is at a low logic level. When disable is at a high logic level, the output becomes a high impedence. In other words, when disable is at a high logic level, it is equivalent to completely removing device M8 from the circuit. ROMs and RAMs are also tri-state devices. Each ROM or RAM must be enabled by a certain logic level at its chip-enable input before the device is capable of inputting or outputting data. In the case of the Page Zero RAMs, this chip-enable input is identified as OD.

4.3 MICROCOMPUTER SYSTEM

The primary function of the Night Driver Microcomputer is to instruct the game circuitry for the proper TV monitor display and audio outputs for corresponding manual inputs.

4.3.1 Program PROMs Enable:

With initial power applied to the Night Driver PCB, the Microprocessor addresses the Program PROMs for an instruction by placing a sixteen-bit code at outputs AB0 through AB15. Enable H2 receives three address lines (AB10, AB11, and AB12) as an instruction of which part of the Program PROMs to access. Outputs of one-of-ten decoder H6 enable

only the individual ROMs of the Program PROMs required for the desired instruction.

4.3.2 Page Zero Enable:

Now, with Enable addressed for the enabling of the desired Program PROMs, and the Program PROMs addressed for a data instruction, the Microprocessor receives an eight-bit data instruction from the Program PROMs on the data bus. If this data instruction includes the storage of information, the Microprocessor addresses Enable one-of-ten decoder J2 (address lines BA9, BA10, and BA11) to enable Page Zero, and it writes data into Page Zero. The procedure of writing into Page Zero is enabled by two signals; output disable OD (pin 9) must be a high logic level and read/write R/$\overline{W}$ (pin 16) must be a low logic level. With this condition, data from the Microprocessor on the data bus is stored into a Page Zero location determined by Page Zero address inputs BA0 through BA7.

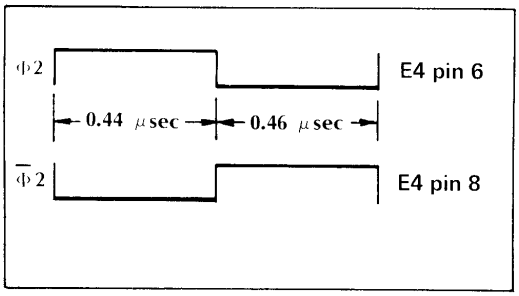


Figure 4-2 Φ2 and $\overline{\Phi 2}$ Signals

4.3.3 Phase 2:

Phase 2 (B0 2) is an output of the Microprocessor and is derived from the 1MHz input signal from divide-by-twelve M3. Phase 2 is the master timing signal of the microcomputer system. The signal, as illustrated in Figure 4-2, is positive when the Microprocessor addresses the Program PROMs for a data instruction.

The Microprocessor addresses Page Zero and writes or reads data when the inversion of phase 2, or phase 2 not (BΦ2), is positive.

4.3.4 Playfield and Roadway Address:

Both the Playfield and Roadway are addressed by the four least significant bits of the address bus from the Microprocessor. However, in order to write data into the Playfield or Roadway RAMs, the latter must receive their enabling signals from Enable J2. Since phase 2 is not an input to Enable J2 (actually C4 pin 5); data is only written into the Playfield and Roadway RAMs when phase 2 not is a low logic level.

4.4 MICROCOMPUTER WATCHDOG

Watchdog is an external monitoring system that resets the Program execution back to its initial instructions, if the program execution deviates from its intended sequence. This is accomplished by a watchdog statement (address code), incorporated in Program Memory (Program PROMs), that results in a $\overline{\text{WATCH-DOG}}$ pulse at the clear inputs of flip-flops L7. This clears the count of vertical blanking pulses ($\overline{\text{V BLANK}}$) and must be accomplished before the flip-flops reach the count of three vertical blanking pulses.

V. INSTALLATION INSTRUCTIONS

5.1 UNPACKING INSTRUCTIONS

5.1.1 Examination for Shipping Damage:

Before shipment from the factory, components and sub-assemblies of each game are carefully checked for proper operation. However, during shipment some adjustments may have changed or parts may have been damaged. Upon initial removal of the game from the shipping container, first examine the exterior of the cabinet. Then open the rear access panel (refer to Section VII, Disassembly and Assembly) and examine the interior of the cabinet. Any shipping damage, such as a dented, cracked or broken cabinet, sub-assemblies broken, loose, etc., should be reported immediately to the shipper and to Atari, Inc.

5.1.2 Mechanical Inspection:

After determination that the game has been received in good condition, carefully inspect the interior parts and verify the following:

(a) All plug-in connectors are firmly seated.

(b) The fuses are all seated in their holders.

(c) No loose foreign objects are present (especially metal objects that could cause electrical short circuits).

(d) No harness wires have become disconnected or pulled loose.

Be sure all major assemblies have been checked: game PCB, the transformer and other components on the electronics tray assembly, the two coin mechanisms, the speakers, player controls, and TV monitor chassis.

Do not go on to the remaining paragraphs in this section until the above mechanical inspection has been thoroughly performed.

5.2 VERIFYING OPERATION OF INTERLOCK SWITCHES:

Interlock switches are located inside the rear access door and are there to prevent accidental shock of anyone who has reason to stick a hand inside the game cabinet. The function of these switches is to remove all power that goes into the game when the rear access door is open. These switches are mechanically aligned by Atari, but it is important that they are checked to insure the proper operation after shipping.

After the completion of subparagraph 5.1.2, plug the AC Power Cord into the appropriate AC Power Source (refer to Section II, Specifications). Set the "Power On/Off" switch, hidden above the accelerator foot pedal, to the "on" position. Within approximately thirty seconds, there should be a raster display on the TV monitor. Verify operation of interlock switches as follows:

(a) Unlock and completely remove rear access door. This will cause the picture of the TV monitor screen to disappear.

(b) Press switch plunger for one of the interlock switches and hold for at least ten seconds. If TV monitor picture comes on, replace the other interlock switch.

(c) Repeat step (b) with the other interlock switch.

(d) Check that both interlock switches are aligned in a manner that when the rear acccess door is opened, the interlock switches will disengage.

Do not go on to the remaining subparagraphs in this section until the operation of the interlock switches has satisfactorily verified.

5.3 OPERATION OF SELF-TEST FEATURE

5.3.1 Activating the Self-Test Feature:

Before activating the Self-Test feature, set the track select switch to the PRO TRACK position and set the gear shifter to the 4th gear position. Now activate the Self-Test feature by unlocking and opening the coin mechanism door, then setting the Self-Test switch located immediately inside and to the left of the coin mechanism door to the "on" position.

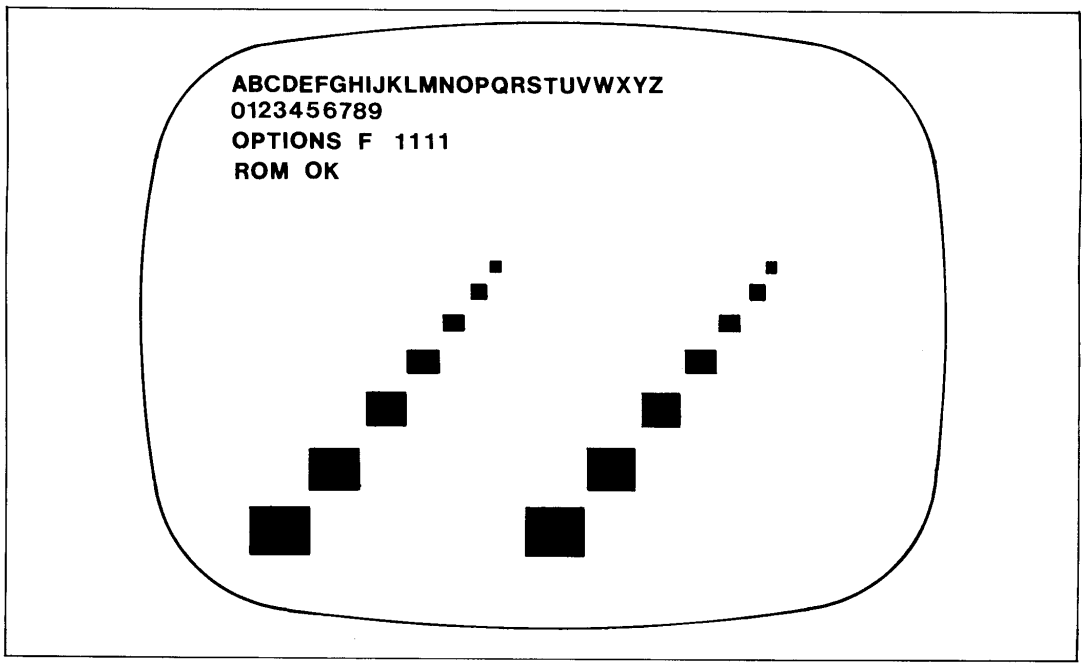


Figure 5-1 Self-Test TV Monitor Display

5.3.2 Visual Check:

The TV monitor viewing screen's display shall be as illustrated in Figure 5-1. The major items of the display to be checked are as follows:

(a) Alphanumerics: Check to make sure that all alphanumerics are displayed in the correct order and each character is complete. Any problems that exist indicate a problem associated with the playfield generator. To troubleshoot, refer to paragraph 5.4 in this section.

(b) Options: At this time, ignore the OPTION line of the TV monitor display. This will be discussed in subparagraph 5.3.4.

(c) ROM Check: The ROM line should indicate a statement "ROM OK". If not the statement will indicate ROM 1 through 7. This number represents the ROM or combination of ROMs that have failed this test. To troubleshoot, refer to paragraph 5.4 in this section.

(d) Roadway Check: The bottom of the TV monitor viewing screen shall display two sets of white boxes that diminish in size from the bottom up and have seven boxes in each group. If these boxes are in any way different than as illustrated in Figure 5-1, refer to paragraph 5.4 in this section.

(e) Steering Check: Turn the steering wheel to the right. The roadway pylon boxes should move to the right. Turn the steering wheel to the left. The roadway pylon boxes should move to the left.

(f) Start Light Check: The start pushbutton should be lighted. If not, refer to paragraph 5.4 in this section.

5.3.3 Audio Check:

Perform the following check steps. If there is a failure, refer to paragraph 5.4 in this section. The following checks should cause an audio screech sound from the game speakers:

(a) Set track select switch to NOVICE TRACK position.

(b) Set track select switch to EXPERT TRACK position.

(c) Press the start pushbutton.

(d) Set gear shifter to 1st-gear position.

(e) Set gear shifter to 2nd-gear position.

(f) Set gear shifter to 3rd-gear position.

(g) Step on the accelerator foot pedal.

(h) Trip the right coin acceptor.

(i) Trip the left coin acceptor.

The following checks should cause *no* audio screech sound from the game speakers:

(j) Set track select switch to PRO TRACK position.

(k) Set gear shifter to 4th-gear position.

5.3.4 Adjusting the Options:

The option line of the TV monitor display indicates the optional game structuring for which the game has been set. These options are adjustable by the owner/operator. For instructions for setting these options, refer to paragraph 3.4 of Section III, Description of Operation.

5.3.5 Game Play Operation Test:

Set the Self-Test switch to the "off" position. Check the operation of the coin mechanisms by inserting old and new coins into the coin slot. Once you determine that the coin mechanisms are OK, initiate game play by pressing the start button. Check that the car motor sound increases while shifting through the gears with the accelerator foot pedal depressed. Then check that there is a crash sound and that the TV monitor display flashes when a roadway pylon makes contact with the car. The game is now ready to earn money.

5.4 TROUBLESHOOTING SELF-TEST FAILURES

5.4.1 Visual Check Failures:

The following subparagraphs (a) through (f) refer to the identical subparagraphs (a) through (f) of paragraph 5.3.2, Visual Check. For example, if there is a failure in the alphanumerics line on the TV monitor display as described in step (a) of subparagraph 5.3.2, troubleshoot by following the hints and instructions in step (a) of this subparagraph. If there is no TV monitor display, check to make sure that the game is plugged into an active AC source, the game is turned on (hidden ON/OFF switch), check all connectors, check all fuses, and check interlock switches. If these are all OK, troubleshoot TV monitor (substitution is best way), then troubleshoot Night Driver PCB (substitution is best way).

(a) Alphanumerics: Replace Night Driver PCB (refer to Section VII). If all of the TV monitor display is garbled, this indicates a problem with the data and/or address lines in the Night Driver PCB. Check that lines are not shorted together or to ground. If TV display is garbled except for boxes at the bottom of the display, there is a malfunction in the Playfield signals. Check these signals using Table 8-1 in Section VIII of this manual as a guide for Circuit familiarization and troubleshooting. Suspect input/output signals of RAM M2 or ROM P2. If alphanumerics line is completely missing, suspect NAND gate J5 or shift register P3 input/output signals.

(b) This step was skipped.

(c) ROM Check: Replace Night Driver PCB (refer to Section VII). If ROM line of the TV monitor display indicates a number instead of OK, then refer to Table 5-1. Find the number that matches the number displayed after the word ROM on the TV monitor display in the FAILURE NUMBER column of Table 5-1. Match that number with the FAILING ROM(s) column. Troubleshoot the ROM circuit(s) indicated in Table 5-1 using Table 8-1 of Section VIII of this manual as a guide for troubleshooting.

Table 5-1 ROM Failures

FAILURE NUMBER	FAILING ROM(s)
1	D1, J1
2	E1, K1
3	D1, E1, J1, K1
4	F1, L1
5	D1, F1, J1, L1
6	E1, F1, J1, L1
7	C1, D1, E1, F1 H1, J1, K1, L1

(d) Roadway Check: Replace Night Driver PCB (Refer to Section VII). If the Roadway display is missing or garbled, there is a malfunction in the Roadway circuits. Check these signals using Table 8-1 of Section VIII of this manual as a guide for circuit familiarization and troubleshooting. If Roadway display is missing, suspect shift register M5 input/output signals, vertical line comparator E7, F7, N7, P7 (pin 8 output), and P8 (pin 6 output), or match latch N3. If garbled, suspect

Roadway RAMs E6, H4, H6, J4, J6, K4, L4, L6, M6, and P6.

(e) Steering Check: If Roadway pylon boxes move in one direction but do not move in the other direction, replace Night Driver PCB. There is a malfunction in the Input Port circuits. Check these signals using Table 8-1 of Section VIII of this manual as a guide for circuit familiarization and troubleshooting. Suspect flip-flop E8 (pin 9 output), multiplexer K9 inputs and outputs, or tri-state device M8 inputs and outputs. If Roadway pylons do not move at all, check continuity of harness wires between Steering PCB and Night Driver PCB. If continuity is OK, check for a voltage that switches between +2 VDC and +5 VDC on pins 4 and 8 of the Steering PCB (referenced to ground) as the steering wheel is very slowly turned. If this voltage is as specified, replace the Night Driver PCB. Suspect flip-flop E8 inputs and outputs, multiplexer K9 inputs and outputs, or tri-state M8. If voltage is not as specified, replace Steering PCB.

(f) Start Light: If start light is not lighted, check for +5 VDC on red wire to Start Switch. If voltage is not present, check continuity of harness wire between switch and Night Driver PCB. If continuity is OK, short black/red wire to Start Switch to ground through a 150-ohm resistor. If still unlighted, replace switch. If lighted, replace Night Driver PCB. Suspect Output Port E5 inputs and outputs or Schmitt trigger J8 (pin 10) output.

5.4.2 Audio Check Failures:

The following subparagraphs (a) through (k) refer to identical subparagraphs (a) through (k) of subparagraph 5.3.3, Audio Check. For example, if there is a failure in step (a) of subparagraph 5.3.3, troubleshoot by following the hints and instructions in step (a) of this subparagraph. If there is no audio sound present in any of the steps in subparagraph 5.3.3, check continuity of white/black wire from gear shifter switches to ground. If continuity is OK, check operation of speakers by substitution. If speakers are OK, replace Night Driver PCB. Suspect Input Port F9 inputs and outputs or tri-state M8.

(a) If no sound, check voltage on red/white wire to the track select switch. If voltage is +5 VDC, replace track select switch. If voltage is 0 VDC, replace Night Driver PCB. Suspect Input Port F9 input.

(b) If no sound, check voltage on white/red wire to the track select switch. If voltage is +5 VDC, replace track select switch. If voltage is 0 VDC, replace Night Driver PCB. Suspect Input Port F9 input.

(c) There should be no audio.

(d) If no sound, check voltage on gray wire to the Start pushbutton. If voltage is +5 VDC, replace Start pushbutton. If voltage is 0 VDC, replace Night Driver PCB. Suspect Input Port F9 input.

(e) If no sound, check voltage on blue/white wire to first gear switch. If voltage is +5 VDC, replace switch. If voltage is 0 VDC, replace Night Driver PCB. Suspect Input Port F9 input.

(f) If no sound, check voltage on yellow/white wire to 2nd-gear switch. If voltage is +5 VDC, replace switch. If voltage is 0 VDC and continuity between switch and Night Driver PCB is OK, replace Night Driver PCB. Suspect Input Port F9.

(g) If no sound, check voltage on orange/white wire to 3rd-gear switch. If voltage is +5 VDC, replace switch. If voltage is 0 VDC and continuity between switch and Night Driver PCB is OK, replace Night Driver PCB. Suspect Input Port F9.

(h) There should be no audio.

(i) If no sound, check voltage on blue wire to accelerator foot pedal. If voltage is +5 VDC, replace switch. If voltage is 0 VDC and continuity between switch and Night Driver PCB is OK, replace Night Driver PCB. Suspect Input Port F9.

(j) If no sound, check voltage on orange wire to coin acceptor switch. If voltage is +5 VDC, replace switch. If voltage is 0 VDC and continuity between switch and Night Driver PCB is OK, replace Night Driver PCB. Suspect Input Port Schmitt trigger E9 (pin 12) output or input of multiplexer F9.

(k) If no sound, check voltage on yellow wire to coin selector switch. If voltage is +5 VDC, replace switch. If voltage is 0 VDC and continuity between switch and Night Driver PCB is OK, replace Night Driver PCB. Suspect Input Port Schmitt trigger E9 (pin 2) output or input of multiplexer F9.

VI. MAINTENANCE AND ADJUSTMENTS

6.1 ROUTINE MAINTENANCE

Due to its solid-state electronic circuitry, this Atari game should require very little maintenance and only occasional adjustment.

Game cabinets and glass may be cleaned with any non-abrasive household cleaner. If desired, special coin machine cleaners which leave no residue can be obtained from distributors.

6.2 ADJUSTMENTS ON TV MONITOR

The TV monitor need be adjusted *only* when the picture is distorted, or if the contrast or brightness seem out of adjustment.

NOTE

The TV monitor is accessible only from inside the game cabinet and these adjustments have to be done while the game is energized. Therefore only persons familiar with safety measures and repair procedures on electrical equipment should perform them.

The monitor's adjustments function like those of a conventional commercial television set, except that the volume adjustment has no effect. Instead the game produces its sound in a speaker separate from the TV monitor. Figure 6-1 shows the location of the adjustments on the rear of the chassis. When making the adjustments follow these general guidelines:

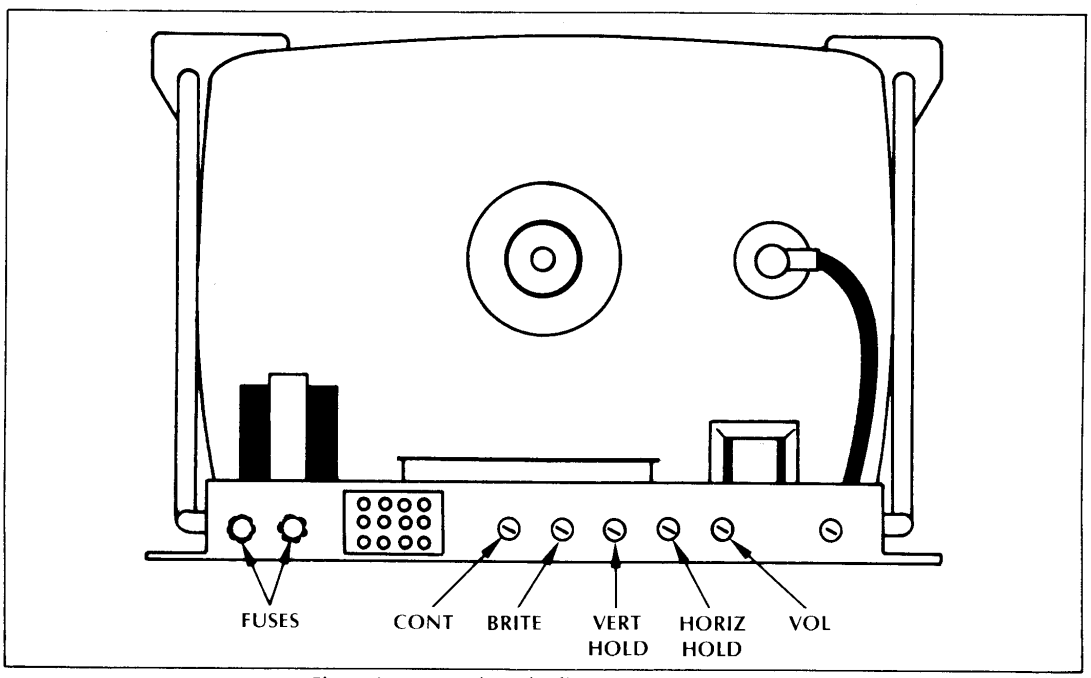


Figure 6-1 Location of Adjustments on TV Chassis

BRITE (Brightness)—Perform this adjustment before the contrast. Adjust so that the white lines covering the screen just barely disappear, when the brightness is turned up.

CONT (Contrast)—Adjust so that the images are as bright as possible against the dark background without being blurred.

HORIZ HOLD (Horizontal Hold)—Adjust if the picture is slightly off-center horizontally, if the images appear warped, or if the picture is broken up into a series of diagonal lines. Adjust for a stable, centered picture.

VERT HOLD (Vertical Hold)—This needs adjustment only if the picture appears to be rolling up or down the screen. Adjust for a stable, centered picture.

VII. DISASSEMBLY AND ASSEMBLY

7.1 GENERAL INFORMATION

The following procedures are supplemented by exploded diagrams 7-1 for the front of the game cabinet and 7-2 for the rear of the game cabinet. All capitalized component terms directly refer to the parts list and drawing A006264-01 located in Section IX of this manual.

When working inside the Rear Door Assembly, always check to make sure that the two interlock switches are not in the defeat position or stuck in the "on" position.

7.2 REMOVING AND INSTALLING THE NIGHT DRIVER PCB

(a) Remove three #8x1¼-inch Flat Head Phillips Screws from each side of the Rear Door Assembly.

(b) Unlock and remove Rear Door Assembly.

(c) Locate R.F. Shield Box Assembly immediately inside the rear access and mounted on the right side panel. It is an aluminum box with many small holes. On the closest end of the box is the R.F. Board Assembly.

(d) Unplug the edge connector from the R.F. Board Assembly.

(e) Remove five #6x½-inch Small Pan Head Phillips Screws from each of the long sides (total of ten) of the R.F. Board Assembly.

(f) Carefully remove the R.F. Board Assembly while pulling the Night Driver PCB out of the R.F. Box Assembly.

(g) To install the Night Driver PCB, follow preceding steps (a) through (f) in the reverse order. *Do not force or bend the printed circuit boards. Before installing them into the R.F. Shield Box Assembly, always inspect the two printed circuit boards for physical damage.*

7.3 REMOVING AND INSTALLING THE TV MONITOR

(a) Remove three #8x1¼-inch Flat Head Phillips Screws from each side of the Rear Door Assembly.

(b) Unlock and remove Rear Door Assembly.

(c) Unplug the 12-pin Molex connector from the chassis of the TV monitor.

(d) With a ⅜-inch wrench, remove two #10-24 Machine Hexagonal Nuts, two #10 Split-Lock Washers, and two #10 Flat Washers from underneath the bottom rear sides of the wood TV Shelf Assembly.

(e) Remove two #10-24x1.25-inch Carriage Bolts from the top rear of the wood TV Shelf Assembly.

(f) With a ⅜-inch wrench, remove four ¼-20 Machine Hexagonal Nuts, four ¼-inch Split Lock Washers, and four ¼-inch flat washers from the rearmost outer edges of the Dashboard Assembly.

(g) From the front of the game cabinet, being careful not to pull on the harness wires, lift the the Dashboard Assembly away from the game cabinet.

(h) Push upwards and pull out the Main Display Plexiglas.

(i) Remove the 23" Monitor Bezel.

(j) Slowly and carefully, slide the TV Shelf Assembly forward and out of the game cabinet.

(k) To install the TV Shelf Assembly, follow preceding steps (a) through (j) in the reverse order. If installing a new TV Shelf Assembly, remove the race car from the screen of the old TV monitor. Attach the race car to the center of the TV monitor screen with the bottom of

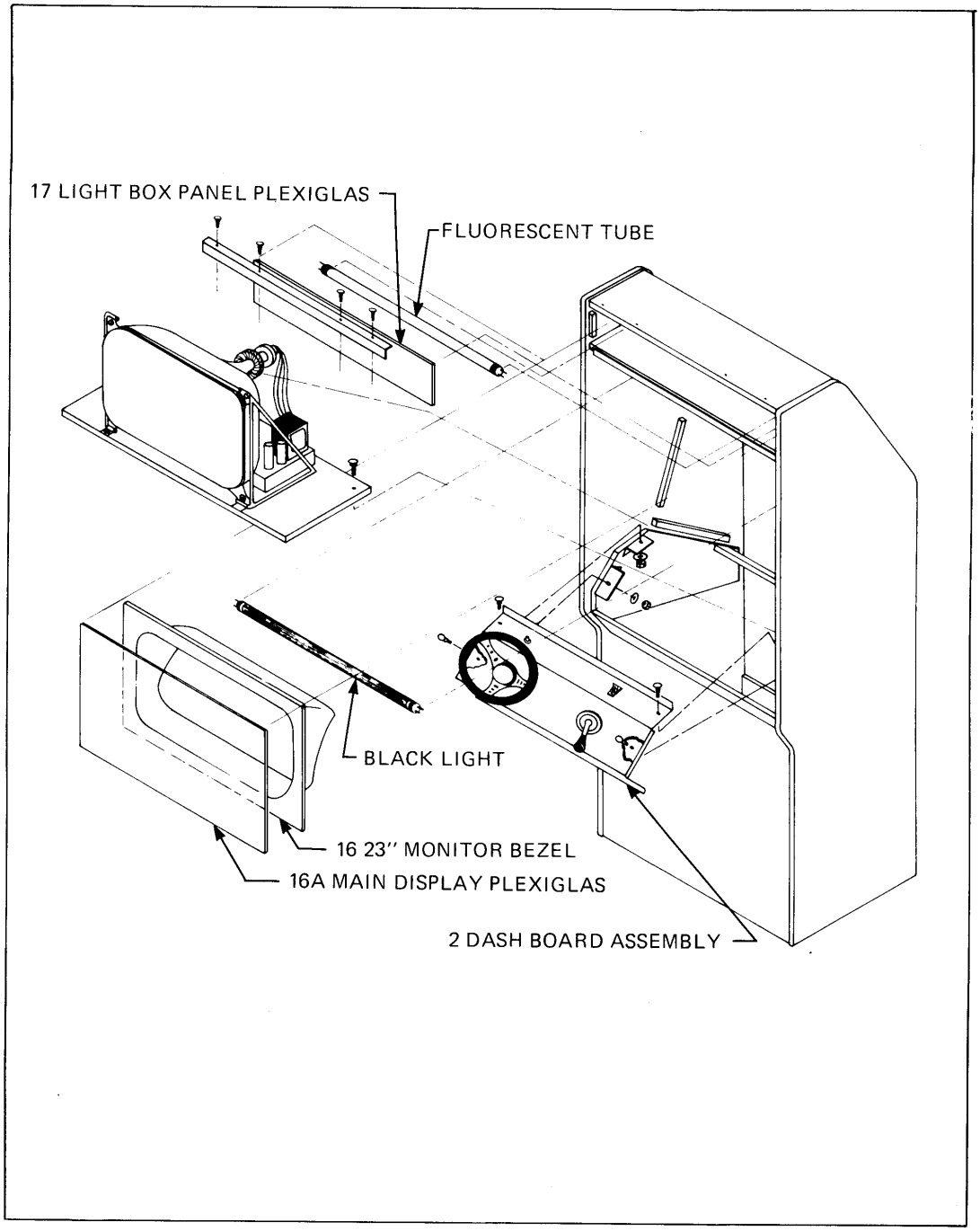


Figure 7-1 Exploded View, Front of Game Cabinet

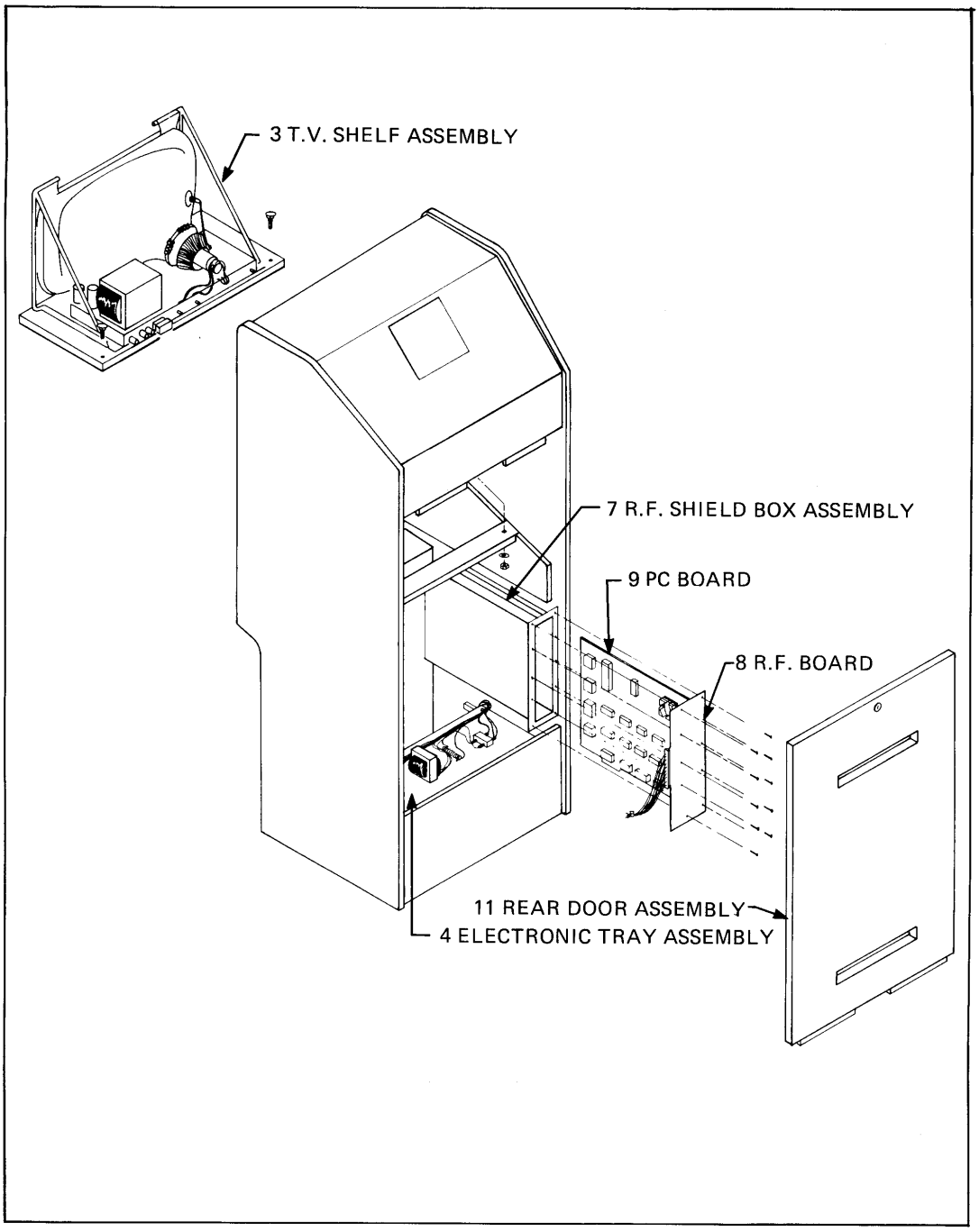


Figure 7-2 Exploded View, Rear of Game Cabinet

the race car ½-inch above the bottom of the screen. Use a water-soluble glue or adhesive tape.

7.4 REPLACING THE STEERING BOARD PCB

(a) Remove three #8x1¼-inch Flat Head Phillips Screws from each side of the Rear Door Assembly.

(b) Unlock and remove Rear Door Assembly.

(c) Unplug the 10-pin Molex connector from the Steering Board PCB.

(d) With a 7/16-inch wrench, remove self-locking hexagonal nut and ¼-inch internal tooth starlock washer from the steering wheel axis screw, while a helper holds the steering wheel at the front of the game cabinet.

(e) Remove black plastic edge-toothed wheel.

(f) Remove Steering Board PCB by removing two #2-56x½-inch Pan Head Phillips Screws.

(g) To install the Steering Board PCB, follow preceding steps (a) through (f) in the reverse order. Before installing the Steering Board PCB, make sure there is a sufficient amount of silicone lubricant on the inner hole of the black plastic edge-toothed wheel.

7.5 REPLACING FLUORESCENT TUBE

(a) With a ⅛-inch hex wrench, remove three #10-32x1-inch Button Head Socket Cap Screws from the top Plexiglas Retainer.

(b) Lift the Attraction Panel Plexiglas up and out of the bottom Plexiglas Retainer.

(c) Remove fluorescent tube.

(d) To install Attraction Panel Plexiglas, follow preceding steps (a) and (b) in the reverse order.

7.6 REPLACING BLACK LIGHT TUBE

(a) Remove three #8x1¼-inch Flat Head Phillips Screws from each side of the Rear Door Assembly.

(b) Unlock and remove Rear Door Assembly.

(c) With a ⅜-inch wrench, remove four ¼-inch flat washers from the back-side outer edges of the Dashboard Assembly.

(d) From the front of the game cabinet, being careful not to pull on the harness wires, lift the Dashboard Assembly away from the game cabinet.

(e) Push upwards and pull out the Main Display Plexiglas.

(f) Remove the 23" Monitor Bezel.

(g) Remove black light.

(h) To reassemble the game cabinet, follow preceding steps (a) through (g) in the reverse order.

VIII. TROUBLESHOOTING AND REPAIR

8.1 GENERAL PROCEDURE

NOTE

This section describes troubleshooting procedures in detail sufficient for a person with moderate technical ability to understand. However, for those interested in gaining more information on video game technology, especially the electronics, we recommend reading the **Video Game Operator's Handbook,** *manual no. TM-043. This book is available from Atari, Inc., attn. Customer Service Dept., 2175 Martin Avenue, Santa Clara, CA 95050 for $5.00 each, or from your distributor.*

8.1.1 Identifying the Trouble Area:

If the Night Driver game fails to respond properly to any of the tests as described in paragraph 5.3 of Section V, Installation Instructions, troubleshoot the game as described in paragraph 5.4. When a failure occurs, you should make certain the failure doesn't exist due to skipping or misreading one of the procedural steps. For failures of the audio checks in subparagraph 5.3.3, it is common sense to first check the associated harness wires using the harness schematic in Section IX of this manual.

The statement "Replace the Night Driver PCB" is intended to eliminate unqualified personnel from damaging this expensive item. The Night Driver PCB is a complicated non-throw-away item and should be only worked on by those who are familiar with its circuitry.

Table 8-1 and Insert 8-1 are a comprehensive familiarity guide to the Night Driver PCB signals. Figure 8-1 is an illustration of the steering signals. All signals of the Night Driver PCB are described in Table 8-1, and many of the signals are illustrated in the figure and insert. For signals to the Playfield and Roadway circuits, the table was written in the same order that the actual hardware receives the signals. The table first covers signals of schematic sheet 1 of the Night Driver PCB; the second sheet, then the third sheet.

8.1.2 Locating the Trouble Cause:

Once a problem has been narrowed down to one or more areas, the next step is to perform various tests and measurements to isolate a specific cause of the trouble. Remember that sometimes a very complicated problem, such as erratic game operation, can be traced to a simple cause—the printed circuit board not being properly seated in its edge connector. Start with the most suspect area and trace backwards from the point where the trouble is first observable, using a process of elimination to eventually locate the faulty component, connection, etc.

Substitution of parts is a legitimate and easy way to isolate the cause. For instance, if the PCB is the suspected trouble area, remove it and substitute a known-to-be-good PCB. Then check for correct game operation. Similarly, to check the TV monitor, connect the game to a known-to-be-good monitor. The harness can often be checked by substitution also. Substitute both a known-to-be-good PCB and TV monitor. If the trouble still persists, the harness must be at fault.

The test equipment for use in troubleshooting is discussed in paragraph 8.2.

8.1.3 Correcting the Trouble Cause:

In practice, the steps required to correct troubles can range from simple adjustments (correctly seating the PCB in its edge connector, changing the setting on a potentiometer, adjusting the picture controls on the TV monitor) to repair of loose connections and replacement of defective parts. Extreme care should be exercised when removing integrated circuit devices and discrete components. Use a 40-watt maximum soldering pencil with a small tip designed especially for IC work. Before removing an IC, clip the signal output or input lead of the suspected failing IC to determine if another component is creating the problem. To remove an IC device, follow this procedure:

> Clip all leads and lift the IC package out, leaving two rows of leads. Then remove leads individually with a soldering iron and needle-nose pliers. Finally, evacuate the holes with a solder sucker. Afterwards

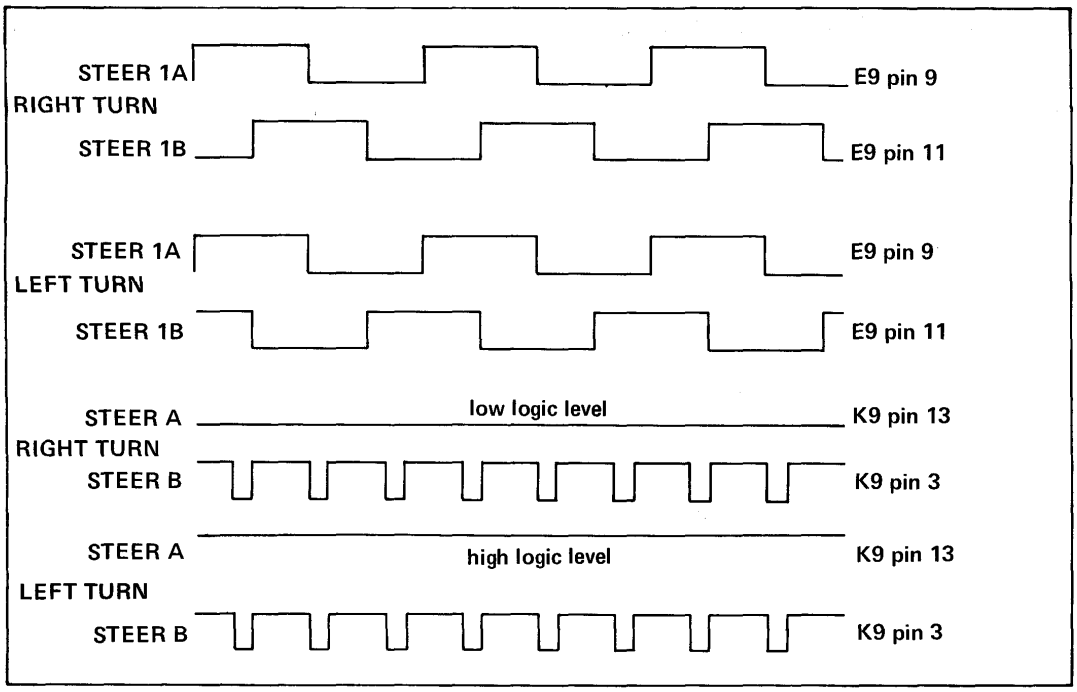


Figure 8-1 Steering Signals

clean the area thoroughly, using an approved PCB cleaning solution to remove any traces of flux and dirt. Alcohol will do in a pinch, if necessary.

The microprocessor, read-only memories, and random-access memories are removed by simply pulling them out of their sockets. When placing them into their sockets, make certain they are placed in the correct socket.

Insert the new IC device using an IC insertion tool, making sure that the reference notch is oriented correctly and that the device's leads are not bent during insertion into the board. Afterwards, be sure to solder each lead on *both* sides of the PCB, using as little solder as possible. After soldering, clean the area thoroughly to remove the flux.

Observe the same removal and insertion procedures when replacing discrete components. Trim the leads as close as possible and be sure to orient diodes and capacitors correctly.

8.1.4 Verifying Correct Game Operation:

After locating and correcting the cause of a trouble, re-energize the game and perform a final check by placing the game in the self-test function, then check for correct operation during game play. Doing this will verify that your troubleshooting was correct. If the game operation is still not correct, go back and double-check your work. Make sure that any replaced components were installed correctly. If this was done properly, then start the troubleshooting steps over again. Keep in mind that there may be more than one trouble at a time, and that correcting one trouble can sometimes bring previously undetectable troubles to light.

This verification is especially important when the original trouble has been intermittent, that is, was not happening all the time.

8.2 TEST EQUIPMENT

Electronic troubleshooting of a video game essentially consists of checking for the presence of various signals and of examining their condition. A

signal can be thought of as acting like a "messenger" that carries instructions from one unit or circuit to another. Many different types of signals are produced in a video game, and for this reason several unusual and perhaps unfamiliar types of test instruments are used during troubleshooting. Each instrument has its own set of advantages and disadvantages for examining a given type of signal, and both the depth of the intended troubleshooting capability and budget will determine what instruments will be needed. Some instruments are basic and essential, no matter what size of service facility, while other optional instruments are desirable because they make troubleshooting easier and quicker.

8.2.1 Basic Test Equipment:

(a) The Video Probe. This is a simple but invaluable instrument having two leads—a test-clip lead and a test-probe lead. During troubleshooting of video signals the test-clip lead is left connected to the test point from resistor R65, located at coordinates P9 of the Night Driver PCB. When the test-probe lead is then connected to any video developmental signal, that signal will be coupled to the video signal going to the TV monitor and a video probe picture will appear on the TV screen. The shape and other characteristics of this picture will give information about the signal being probed. The video probe is suited for troubleshooting synchronization and image signals, but will not be useful for extremely fast signals (such as the clock) or for very slow analog or digital signals.

A video probe can be constructed in a few minutes from these common electrical components: a length of 20 AWG (American Wire Gauge) rubber-coated wire, a 4.7K-ohm, ¼-watt carbon resistor, and two test leads. For the leads, use a single Mouser test clip (Mouser #131C301 or 302) attached to one end of the wire, and a test prod containing the resistor on the other.

To assemble the video probe, proceed as follows: Remove the cap from the test clip and strip 3/16 inch off each end of the wire. Solder one end to the post in the test clip, thread the other end through the hole in the cap, and snap on the cap. Next unscrew the plastic body of the test prod from the point and trim both leads of the resistor to a 3/16-inch length. Solder one resistor lead to the inside of the point. Thread the other end of the wire through the hole in the body and solder it to the other resistor lead; screw the body back onto the point.

(b) The Logic Probe. This is a test instrument designed for fast verification of digital IC outputs. It is small, convenient to carry, easy to read, and relatively inexpensive. The logic probe derives its power from the system under test; it has two power leads, one for connection to ground and the other to +5 volts DC. When the logic probe's tip is held against a digital signal point, three colored lamps in the tip will indicate the signal's condition or state, as follows:

- The red lamp lit indicates a high or logic level 1 (for TTL components, this is +2.4 to +5 volts)
- The white lamp lit indicates a low or logic 0 (for TTL components, this is 0 to +0.8 volt)
- The blue lamp lit indicates that the signal is changing states
- No lamps lit indicate the grey region between 0 and 1 (for TTL this is between +0.8 and +2.4 volts)

A circuit shorted to ground will illuminate the white lamp and an open circuit will illuminate the red lamp.

The logic probe is readily available from electronic supply sources; a commercial model found satisfactory is the Kurz-Kasch model LP 520.

(c) The Logic Pulser. This test instrument is similar in size and shape to the logic probe, and it also derives its power from the system under test. When the logic pulser's tip is held against a digital signal point, the source and sink capabilities of the pulser override any IC output, and the point is driven to the opposite logic level. If the point that the logic pulser is held against is low, pressing the switch on the side of the pulser will introduce a high pulse. Conversely, pulsing a high line will pull that line low momentarily.

During troubleshooting the logic pulser allows stimulation of in-circuit ICs with a shaped digital pulse. For example, a certain feature of the game may not be working and you suspect that a circuit is not receiving the necessary signal. Use the pulser to imitate that signal: if the circuit begins working, you have proved that the signal was in fact missing and you can begin tracking it down. This technique is very similar to jumping coils in electromechanical games such as pinball machines.

In addition to the regular "pulse" button, there is another switch mounted on the logic pulser. When this switch is set in the "rep" mode, the instrument pulses the digital signal point at a 5-Hz rate or 5 times per second. This extremely low rate is slow enough to allow watching events initiated by the pulser. Counter outputs, for example, are more easily observed when the counter is pulsed or clocked at this rate.

The logic pulser is also readily available from electronic supply sources; a commercial model found satisfactory is the Kurz-Kasch model HL 583.

(d) Oscilloscope. The most versatile test instrument, and also the most expensive, is the oscilloscope. The high-speed TTL integrated circuits used in video games produce fast-rise-time signals. The oscilloscope should have a 50-MHz bandwidth, dual trace and dual time base capability. These latter features allow examination of both input and output signals simultaneously, so that precise timing relationships can be checked. The oscilloscope should also have provision for internal or external sync.

Of the newer, solid-state oscilloscopes, a satisfactory model is the Tektronix 465.

(e) VOM or Volt-Ohmmeter. This common measuring instrument is extremely useful in video game troubleshooting. It can be used to check line voltage, transformer secondary windings, continuity, resistance, power supply voltages, and to some extent used for measurements in the analog circuitry.

One commercial model found satisfactory is the Simpson 260.

8.2.2 Optional Test Equipment:

(a) The Logic Comparator. This test instrument's main benefit is that it can be used to check the functioning of an integrated circuit device while the device is still in place on the printed circuit board. The logic comparator performs the check by comparing the suspect ICs functioning with that of an identical-type reference IC mounted in the instrument itself. Suppose that the functioning of a type-74195 device on the PCB is suspected to be defective. First insert a program card with a known-to-be-good 74195 into the logic comparator, and then clip the comparator test leads onto the leads of the suspect device. If there are any logic state differences between the reference IC and the suspect IC under test, then a LED on the logic comparator will light up to indicate which output is not functioning correctly. Once a defective IC has been located, it should be replaced.

Logic comparators are readily available from electronic supply sources.

(b) Atari Universal Test Fixture. In situations where a large number of video games are being serviced, investment in the Universal Test Fixture will be justified. This item of test equipment forms a test station for troubleshooting printed circuit boards after they have been removed from the game cabinet. The Universal Test Fixture has a full set of controls for operating the game and also has its own TV monitor. The game's PCB is plugged into an edge connector mounted on the side of the Fixture; with this arrangement the PCB is positioned in a convenient way for connecting probes and other test instruments.

A program and card inserted into a receptacle in the top of Fixture takes the place of the game's interconnect wires. The program card thus sets up the Fixture for each particular game; the game's name is clearly printed on the program card itself.

With the Universal Test Fixture the method of troubleshooting via substitution of known-to-be-good parts is made fast and convenient. For example, suppose that the TV picture in a game is completely broken up and you want to determine whether the game or monitor is causing the problem. Remove the PCB and plug it into the Fixture's edge connector, and also insert the correct program card for that game. If the picture on the Fixture's monitor is correct, then you know that the problem lies in the game's monitor.

8.3 SPECIFIC TROUBLESHOOTING INFORMATION

The following subparagraphs give additional troubleshooting information about certain areas of the Night Driver game.

8.3.1 Coin Mechanism:

If a player inserts a coin and the game does not respond, first check the coin mechanism. If pressing the coin rejector button forces the rejector mechanism to return the coin, then examine the coin to make sure that it is genuine. If it is, then use a set of your own test coins (which should include both very new and very old, worn coins) to determine whether or not the player's coin is undersize or underweight. If your test coins are also returned, this indicates that servicing of the coin acceptor portion of the coin mechanism is called for. Generally the cause of this particular problem is an improperly adjusted magnet gate.

Inside the coin mechanism a magnet is used to test the metallic composition of the coin. Highly magnetic coins, such as those made of steel or iron, will be retained by the magnet and can be returned by actuating the wiper operating lever. Coins having comparatively high magnetic properties will be slowed down by the magnet, and will drop off the end of the rail short of "accept" entrance and be returned.

Coins having little or no magnetic properties, such as brass or zinc coins, will pass through the magnetic field so fast that they will overshoot the "accept" entrance and be returned.

A magnetic gate adjusted with too large a gap may pass both genuine and counterfeit coins. An adjustment with too small a gap can lead to rejection of some or even all coins. Over a period of time, the screw that adjusts the magnet gate has a tendency to work loose, resulting in a gradual narrowing of the gate. At first, only the thickest (i.e., newest) coins are rejected. As time passes, more and more coins are rejected until finally player complaints lead to the calling of the game repairman.

If pressing the coin rejector button does not cause the coin to be returned, and if the game still does not respond, then check the coin mechanism to see if the coin is jammed inside.

If you are certain that the coin is genuine, and that the coin passes through the coin mechanism and into the cash box, then the lack of game response is probably due to some kind of electrical trouble. Check for signals at the electrical contacts of the coin mechanism before moving on to the harness and other parts of the circuitry.

8.3.2 TV Monitor:

The TV monitor is a self-contained unit housed in its own chassis. A trouble's cause may be narrowed down to the monitor—either by the substitution method using a known-to-be-good monitor, or by verifying presence of AC power to the monitor power supply and presence of the *correct* composite video signal. The entire monitor can then be removed from the game cabinet. Doing this facilitates troubleshooting steps, because all monitor components will then be accessible.

A schematic diagram of the monitor circuitry is included in section IX of this manual. After disconnecting and removing the monitor from the game, standard TV troubleshooting techniques are adequate for locating causes of trouble. Additional servicing information is available from the monitor manufacturer (Motorola).

Table 8-1 Night Driver Signal Descriptions

AUDIO SIGNALS

SCHEMATIC SIGNAL	FROM	TO	SIGNAL DESCRIPTION
ATTRACT	E5 (pin 5)		High logic level during attract mode. From output port E5. Disable Motor Sound.
BANG	Summing point of resistors	BANG input resistor R61 of Audio Amplifier A9.	BANG sound that is the result of a roadway pylon making contact with the car.
$\overline{\text{CRASH}}$	E5 (pin 22)	D6 (pin 9) D7 (pin 9)	Low logic level from Output Port E5 that resets noise generator D6, D7.
		C8 (pin 11) D8 (pin 13)	Low logic level from Output Port E5 that enables BANG generator C8, D8.
MOTOR SOUND		MOTOR input resistor R60 of Audio Amplifier A9.	Summed and modulated frequencies that depend upon the digital $\overline{\text{SPEED}}$ input of the motor generator.
SPEED 1 SPEED 2 SPEED 3 SPEED 4	D5 (pin 2) D5 (pin 5) D5 (pin 7) D5 (pin 10)	Resistor R11 Resistor R10 Resistor R9 Resistor R8	Digital SPEED information from output port D5 that is converted into analog by summing resistors R8, R9, R10, and R11. Analog signal controls the oscillating frequency of oscillators A5, A6, and A7.
SCREECH 1	C7 (pin 11)	Screech 1 input resistor R59 of Audio Amplifier A9.	Screech audio signal of approximately 1KHz modulated by digital noise and gated through NAND gate C7 with SKID 1 signal.
SCREECH 2	C2 (pin 3)	Screech 2 input resistor R58 of Audio Amplifier A9.	Screech audio signal of approximately 833 Hz modulated by digital noise and gated through NAND gate C7 with SKID 2 signal.
SKID 1	D5 (pin 12)	C7 (pin 13)	Enabling signal for SCREECH 1 audio signal. From Output Port D5.
SKID 2	D5 (pin 15)	C7 (pin 1)	Enabling signal for SCREECH 2 audio signal. From Output Port D5.
AUDIO OUTPUT (SPEAKER)	minus side of 1000 μf Cap, C14.	Speakers	Audio output from audio amplifier A9.

INPUT PORTS SIGNALS

$\overline{\text{ACC}}$	Accelerator Switch	Edge Connector Pin P F9 (pin 1)	Low logic level to F9 when accelerator foot pedal is depressed. Transferred to output of F9 only if address input is as follows: BA0—high logic level BA1—low logic level BA2—high logic level
$\overline{\text{GEAR 1}}$	Gear shifter 1st gear Switch	Edge Connector Pin H M9 (pin 12)	Low logic level to M9 when gear shifter is in 1st gear position. Transfers to output 2Y only if address input is as follows:

SCHEMATIC SIGNAL	FROM	TO	SIGNAL DESCRIPTION
			BA0 —low logic level BA1—high logic level
$\overline{\text{GEAR 2}}$	Gear shifter 2nd gear Switch	Edge Connector Pin F M9 (pin 4)	Low logic level to M9 when gear shifter is in 2nd gear position. Transfers to output 1Y only if address input is as follows: BA0 —low logic level BA1—high logic level
$\overline{\text{GEAR 3}}$	Gear shifter 3rd gear Switch	Edge Connector Pin K K9 (pin 12)	Low logic level to K9 when gear shifter is in 3rd gear position. Transfers to output 2Y only if address input is as follows: BA0 —low logic level BA1—high logic level
OPT1 OPT2 OPT3 OPT4	L10 (pin 15) L10 (pin 14) L10 (pin 6) L10 (pin 7)	M9 (pin 10) M9 (pin 6) K9 (pin 10) K9 (pin 6)	Logic input to 1C0 and 2C0 inputs of multiplexers K9 and M9. Transfers to 1Y and 2Y only if address input is as follows: BA0 —low logic level BA1—low logic level Logic level inputs of OPT1 through OPT4 for given setting of hexadecimal switch L10 as follows:
$\overline{\text{START}}$	START push-button	Edge Connector Pin 13 F9 (pin 2)	Low logic level to F9 when START pushbutton is depressed. Transfers to output of F9 if address input is as follows: BA0 —low logic level BA1—high logic level BA2—low logic level

Switch Setting	OPT1	OPT2	OPT3	OPT4
0	low	low	low	low
1	high	low	low	low
2	low	high	low	low
3	high	high	low	low
4	low	low	high	low
5	high	low	high	low
6	low	high	high	low
7	high	high	high	low
8	low	low	low	high
9	high	low	low	high
A	low	high	low	high
B	high	high	low	high
C	low	low	high	high
D	high	low	high	high
E	low	high	high	high
F	high	high	high	high

SCHEMATIC SIGNAL	FROM	TO	SIGNAL DESCRIPTION
STEER A	E8 (pin 9)	K9 (pin 13)	Steering direction input to multiplexer K9. Low logic level indicates right turn. High logic level indicates left turn. Transfers to output 2Y of K9 if address input is as follows: BA0 —high logic level BA1—high logic level Refer to Figure 8-1.
STEER 1A	Steering Board Assembly pin 8	Edge Connector Pin S E9 (pin 9)	Steering input from Steering Board Assembly. Leads STEER 1B for right turn. Lags STEER 1B for left turn. Refer to Figure 8-1.
STEER B	E8 (pin 5)	K9 (pin 3)	Steering rate input (the faster steering wheel is turned, the shorter the duty cycle of the pulse input) to multiplexer K9. Transfers to output 1Y of K9 if address input is as follows: BA0 —high logic level BA1—high logic level Refer to figure 8-1.
STEER 1B	Steering Board Assembly pin 4	Edge Connector Pin 16 E9 (pin 11)	Steering input from Steering Board Assembly. Lags STEER 1A for right turn. Leads STEER 1A for left turn. Refer to Figure 8-1.
$\overline{\text{TEST}}$	TEST Switch	Edge Connector Pin J K9 (pin 5)	Low logic level to K9 when TEST Switch is set to "on" position. Transfers to output of K9 if address input is as follows: BA0 —high logic level BA1—low logic level
TRACK SELECT 1	track select Switch	Edge Connector Pin 14 F9 (pin 15)	Low logic level to F9 when track select switch is set to NOVICE TRACK position. Transfers to output of F9 only if address input is as follows: BA0 —low logic level BA1—low logic level BA2—high logic level
TRACK SELECT 2	track select Switch	Edge Connector Pin R F9 (pin 14)	Low logic level to F9 when track select switch is set to PRO TRACK position. Transfers to output of F9 only if address input is as follows: BA0 —high logic level BA1—low logic level BA2—high logic level
V BLANK	J7 (pin 10)	K9 (pin 11)	V BLANK pulse transfers from the input to the output of K9 only if address input is as follows: AB0 —high logic level AB1—low logic level Refer to Insert 8-1.

OUTPUT PORTS SIGNALS

SCHEMATIC SIGNAL	FROM	TO	SCHEMATIC SIGNAL
BD0	F3 (pins 2 & 4)	D5 (pin 3)	$\overline{\text{SPEED 1}}$ logic level same as BD0 logic level when OUT0 goes from low logic level to high logic level.
BD1	E3 (pins 12 & 14)	D5 (pin 4)	$\overline{\text{SPEED 2}}$ logic level same as BD1 logic level when $\overline{\text{OUT0}}$ goes from low logic level to high logic level.
BD2	E3 (pins 2 & 4)	D5 (pin 6)	$\overline{\text{SPEED 3}}$ logic level same as BD2 logic level when $\overline{\text{OUT0}}$ goes from low logic level to high logic level.
BD3	F3 (pins 5 & 7)	D5 (pin 11)	$\overline{\text{SPEED 4}}$ logic level same as BD3 logic level when $\overline{\text{OUT0}}$ goes from low logic level to high logic level.
BD4	F3 (pins 12 & 14)	D5 (pin 13)	SKID 1 logic level same as BD4 logic level when $\overline{\text{OUT0}}$ goes from low logic level to high logic level.
BD5	E3 (pins 9 & 11)	D5 (pin 14)	SKID 2 logic level same as BD5 logic level when $\overline{\text{OUT0}}$ goes from low logic level to high logic level.
BD0	F3 (pins 2 & 4)	E5 (pin 3)	$\overline{\text{CRASH}}$ logic level same as BD0 logic level when $\overline{\text{OUT1}}$ goes from low logic level to high logic level.
BD1	E3 (pins 12 & 14)	E5 (pin 4)	ATTRACT logic level same as BD1 logic level when $\overline{\text{OUT1}}$ goes from low logic level to high logic level.
BD2	E3 (pins 2 & 4)	E5 (pin 6)	Output not used.
BD3	F3 (pins 5 & 7)	E5 (pin 11)	Logic level at N9 (pin 1) same logic level as BD3 when $\overline{\text{OUT1}}$ goes from low logic level to high logic level.
BD4	F3 (pins 12 & 14)	E5 (pin 13)	Logic level as J8 (pin 11) same logic level as BD4 when $\overline{\text{OUT1}}$ goes from low logic level to high logic level.
BD5	E3 (pin 9 & 11)	E5 (pin 14)	Output not used.

MICROPROCESSOR SIGNALS

AB0	C3 (pin 9)	C2 (pin 2)	Address bus to 8T97 tri-state devices. Tri-state devices not used for high Z output, but instead only used as signal buffer.
AB1	C3 (pin 10)	C2 (pin 4)	
AB2	C3 (pin 11)	C2 (pin 6)	
AB3	C3 (pin 12)	C2 (pin 10)	
AB4	C3 (pin 13)	C2 (pin 12)	
AB5	C3 (pin 14)	C2 (pin 14)	
AB6	C3 (pin 15)	B2 (pin 2)	
AB7	C3 (pin 16)	B2 (pin 4)	
AB8	C3 (pin 17)	B2 (pin 6)	
AB9	C3 (pin 18)	B2 (pin 10)	
AB10	C3 (pin 19)	B2 (pin 12)	
AB11	C3 (pin 20)	B2 (pin 14)	
AB12	C3 (pin 22)	B4 (pin 10)	
AB13	C3 (pin 23)	B4 (pin 12)	
AB14	C3 (pin 24)	B4 (pin 4)	
AB15	C3 (pin 25)	B4 (pin 6)	

SIGNAL	From/To	From/To	SIGNAL DESCRIPTION
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	C3 (pin 33) C3 (pin 32) C3 (pin 31) C3 (pin 30) C3 (pin 29) C3 (pin 28) C3 (pin 27) C3 (pin 26)	F3 (pin 3) E3 (pin 13) E3 (pin 3) F3 (pin 6) F3 (pin 13) E3 (pin 10) E3 (pin 6) F3 (pin 10)	Bi-directional data bus to bi-directional buffers 8T28. Data buffers E3 and F3 buffer the data signal from the Microprocessor through one path of E3 and F3 when R/W is low logic level and buffer the data signal to the Microprocessor through another path when R/$\overline{W}$ is a high logic level.

MICROPROCESSOR SIGNALS (CONT)

SIGNAL	FROM	TO	SCHEMATIC SIGNAL
$\overline{IRQ}$	J7 (pin 14)	C3 (pin 4)	Interrupt request. This signal informs the Microprocessor that the vertical blanking period is beginning. Refer to Insert 8-1.
RESET	C7 (pin 6)	C3 (pin 40)	This signal is the result of watchdog. Refer to Section IV, Theory of Operation, paragraph 4.4.
R/W	C3 (pin 34)	B4 (pin 14)	Read/write signal is a Microprocessor signal derived from phase 2 and determines the direction of data to or from the Microprocessor.
$\Phi 2$	C3 (pin 39)	E4 (pin 9)	Phase 2: Basic timing signal of the Microprocessor. Refer to Section IV, Theory of Operation, subparagraph 4.3.3.

WATCH DOG SIGNALS

V BLANK WATCH DOG RESET	J7 (pin 11) K7 (pin 9) C7 (pin 6)	L7 (pin 11) L7 (pins 1 & 13) C3 (pin 40)	The V $\overline{BLANK}$ pulse starts L7 to flip-flop. After three pulses a low logic level will appear at $\overline{RESET}$. However, this should never happen if the Micorprocessor address bus and read/write bus (BR/$\overline{W}$) and Program Memory is operating properly. Program Memory instructs an address that is decoded by Enable J2 for an output of $\overline{HFC}$ (J2 pin 3). At the same time, the Microprocessor outputs a low logic level BR/$\overline{W}$. These two signals are received by Decoder K7 (schematic sheet 3) through OR gate K8. The result is a low logic $\overline{WATCH\text{-}DOG}$ signal at the output of K7 (pin 9). If all is operating properly, $\overline{WATCH\text{-}DOG}$ will be present before flip-flop L7 reaches the count of three pulses.

PLAYFIELD SIGNALS (cont)

SCHEMATIC SIGNAL	FROM	TO	SIGNAL DESCRIPTION
BA0	C2 (pin 3)	L2 (pin 13)	During V BLANK period (V BLANK is a high logic level), BA0 through BA6 address the Playfield RAM through multiplexers K2 and L2. Also BR/$\overline{W}$ is transferred through multiplexer K2. If BR/$\overline{W}$ is a low logic level, data is written into the Playfield RAM via the Data Bus.
BA1	C2 (pin 5)	L2 (pin 10)	
BA2	C2 (pin 7)	L2 (pin 6)	
BA3	C2 (pin 9)	L2 (pin 3)	
BA4	C2 (pin 11)	K2 (pin 13)	
BA5	C2 (pin 13)	K2 (pin 10)	
BA6	B2 (pin 3)	K2 (pin 6)	
BR/W	B4 (pin 13)	K2 (pin 3)	During $\overline{\text{V BLANK}}$ period (V BLANK is a low logic level), 8H through 128H, 16V, and 32V address the Playfield RAM through multiplexers K2 and L2. The read/write input of the Playfield RAM becomes a high logic level (K2 1A input transferred to 1Y output); thus the data written into the Playfield RAM during V BLANK period is now addressed (resulting in transferring the data to address the Playfield ROM) by horizontal and vertical timing signals.
8H	L3 (pin 14)	L2 (pin 14)	
16H	L3 (pin 13)	L2 (pin 11)	
32H	L3 (pin 12)	L2 (pin 5)	
64H	L3 (pin 11)	L2 (pin 2)	
128H	J3 (pin 14)	K2 (pin 14)	
16V	H8 (pin 14)	K2 (pin 11)	
32V	H8 (pin 13)	K2 (pin 5)	
$\overline{\text{PFW}}$	J2 (pin 2)	D4 (pin 1)	During V BLANK period all three signals would normally be high until Enable H2 receives an address that results in a low logic level $\overline{\text{PFW}}$ signal. At this time there will be a high logic level output from NOR gate D4 (pin 12). This high logic level input to M2 (pin 10) enables the tri-state data buffers of M2 to receive a data input. Refer to Insert 8-1.
$\overline{\text{PFR}}$	H2 (pin 1)	D4 (pin 2)	
V BLANK	J7 (pin 10)	D4 (pin 13)	
$\overline{\text{PFW}}$	J2 (pin 2)	M1 (pins 1 & 15)	Low logic level $\overline{\text{PFW}}$ signal enables tri-state device M1 so data may be written into the Playfield RAM M2.
1V	F8 (pin 14)	P2 (pin 21)	These three signals are the three least significant bits of the Playfield ROM address. These bits determine which horizontal line is to be scanned with what ROM data.
2V	F8 (pin 13)	P2 (pin 22)	
4V	F8 (pin 12)	P2 (pin 23)	
1H	K3 (pin 13)	J5 (pin 1)	These eight signals determine when Shift Register P3 loads data for displaying a character. Signals $\overline{\text{V BLANK}}$ and 256H determine that P3 will be loaded only during the horizontal scan period. Signals $\overline{8V}$, $\overline{64V}$, and $\overline{128V}$ determine that P3 is loaded during horizontal scan lines zero through eight, sixteen through twenty-four, thirty-two through forty, and forty-eight through fifty-six. Signals 1H, 2H, and 4H determine that P3 is loaded thirty-two times per enabled scan line.
2H	K3 (pin 12)	J5 (pin 4)	
4H	K3 (pin 11)	J5 (pin 5)	
256H	J3 (pin 13)	J5 (pin 11)	
$\overline{\text{V BLANK}}$	J7 (pin 11)	J5 (pin 6)	
$\overline{8V}$	L8 (pin 2)	J5 (pin 3)	
$\overline{64V}$	J8 (pin 4)	J5 (pin 2)	
$\overline{128V}$	J8 (pin 8)	J5 (pin 12)	

SCHEMATIC SIGNAL	FROM	TO	SIGNAL DESCRIPTION
6MHz	K3 (pin 14)	P3 (pin 7)	When a low logic level pulse appears on load input of P3 (pin 15), the data input from the Playfield ROM is immediately clocked out as serial data from P3 (pin 13) at the rate of 6MHz.
PLAYFIELD	P3 (pin 13)	K8 (pin 5)	Playfield video serial data generated by the Playfield circuitry.

ENABLE SIGNALS

BA10 BA11 BA12 BΦ2 BA15	B2 (pin 11) B2 (pin 13) B4 (pin 9) E4 (pin 6) B4 (pin 7)	H2 (pin 15) H2 (pin 14) H2 (pin 13) F4 (pin 10) F4 (pin 9)	These five signals enable the read address decoder H2. If BΦ2 or BA15 is a low logic level, there will not be an output from Enable H2. The Enable outputs for a given input are as follows:

BA15	BΦ2	BA12	BA11	BA10	H2 Output Signal	H2 Pin #
H	H	L	L	L	$\overline{\text{PFR}}$	pin 1
H	H	L	L	H	$\overline{\text{STEER RESET}}$	pin 2
H	H	L	H	L		pin 3
H	H	L	H	H		pin 4
H	H	H	L	L	$\overline{\text{PROM 0}}$	pin 5
H	H	H	L	H	$\overline{\text{PROM 1}}$	pin 6
H	H	H	H	L	$\overline{\text{PROM 2}}$	(pin 7)
H	H	H	H	H	$\overline{\text{PROM 3}}$	(pin 9)

BA9 BA10 BA11 BA12 BΦ2 BA13 BA14 BA15	B2 (pin 9) B2 (pin 11) B2 (pin 13) B4 (pin 9) E4 (pin 8) B4 (pin 11) B4 (pin 5) B4 (pin 7)	J2 (pin 15) J2 (pin 14) J2 (pin 13) D4 (pin 3) E4 (pin 11) C4 (pin 5) C4 (pin 6) C4 (pin 9) C4 (pin 8)	These eight signals enable address decoder J2. If BA12, BΦ2, BA13, BA14, or BA15 is a high logic level, there will not be an output from Enable J2. The Enable output for a given input is as follows:

BA15	BA14	BA13	BΦ2	BA12	BA11	BA10	J2 Output Signal	J2 pin #
L	L	L	L	L	L	L	$\overline{\text{SCRAM}}$	pin 1
L	L	L	L	L	L	H	$\overline{\text{PFW}}$	pin 2
L	L	L	L	L	H	L	$\overline{\text{HVC}}$	pin 3
L	L	L	L	L	H	H	$\overline{\text{IN 0}}$	pin 4
L	L	L	L	H	L	L	$\overline{\text{IN 1}}$	pin 5
L	L	L	L	H	L	H	$\overline{\text{OUT 0}}$	pin 6
L	L	L	L	H	H	L	$\overline{\text{OUT 1}}$	pin 7
L	L	L	L	H	H	H	*not used*	pin 9

POWER SUPPLY VOLTAGES

SCHEMATIC SIGNAL	FROM	TO	SIGNAL DESCRIPTION
P	Resistors R1, R7, R48, R52 and R112	many locations	The symbol "P" stands for pull-up. This means that anywhere on the schematic that the symbol "P" appears, that point is connected directly to resistors R1, R7, R48, R52 and R112. Therefore the circuit is "pulled-up" to +5 VDC one of those pull-up resistors.
+5V	LM323	many locations	This is the +5 VDC power to all integrated circuits on the PCB, except Audio Amplifier A9.
+20V (DC, unreg)	Plus side of 4700 μfd cap. C27.	A9 (pins 9 & 11)	This is the +20 VDC unregulated power for the Audio Amplifier.

VIDEO SIGNALS

$\overline{\text{H SYNC}}$ $\overline{\text{V SYNC}}$	H5 (pin 6) J7 (pin 6)	P8 (pin 9) P8 (pin 10)	These two signals are the horizontal and vertical sync signals necessary to "kick" the TV monitor scanning circuitry into a retrace. $\overline{\text{H SYNC}}$ is inverse of $\overline{\text{H SYNC}}$ and $\overline{\text{V SYNC}}$ is inverse of $\overline{\text{V SYNC}}$, as illustrated in Insert 8-1.
256H $\overline{\text{V BLANK}}$	J3 (pin 13) J7 (pin 11)	P8 (pin 2) P8 (pin 1)	These two signals are the horizontal and vertical blanking pulses necessary to drive the TV monitor into the black level during retrace. The combination of these two signals is COMP B at P8 (pin 3). Refer to Insert 8-1.
ROADWAY PLAYFIELD	L8 (pin 6) P3 (pin 13)	K8 (pin 4) K8 (pin 5)	These two signals are the video serial data from the Playfield circuitry and the Roadway circuitry. The playfield consists of four possible horizontal rows of alpha numerics between horizontal scan lines zero and eight, sixteen and twenty-four, thirty-two and forty, and forty-eight and fifty-six. The Roadway consists of the fourteen roadway pylons.
VIDEO INVERT	C8 (pin 3)	C6 (pin 9)	This signal is present anytime the roadway makes connection with the car. The signal is originated in the audio BANG circuit. Its function is to make the TV monitor display flash during the BANG sound period.
8V 16V 32V 64V	F8 (pin 11) H8 (pin 14) H8 (pin 13) H8 (pin 12)	C4 (pin 2) C4 (pin 3) N8 (pin 3) N8 (pin 2)	These signals provide a backlight window at the center bottom of the TV monitor display. Signal $\overline{\text{V BLANK}}$ places the window on the TV monitor display during the horizontal scan time. The

SCHEMATIC SIGNAL	FROM	TO	SIGNAL DESCRIPTION
PSA1 PSA2 PSA3 PSA4	L2 (pin 12) L2 (pin 9) L2 (pin 7) L2 (pin 4)	P5 (pin 3) P5 (pin 6) P5 (pin 10) P5 (pin 13)	Picture sync/address signals. These signals are the address signals for the vertical position RAM (H6, P6), horizontal position RAM (J6, L6), and character RAM (E6, M6). During the vertical blanking period, the address signal comes directly from the four least significant bits of the address bus (BA0 through BA3, inputs L2 pins 13, 10, 6, and 3). During the vertical non-blanking period and during horizontal blanking, the address signal comes directly from horizontal synchronization 8H, 16H, 32H, and 64H (inputs L2 pins 2, 5, 11, and 13).
VP1 VP2 VP3 VP4 VP5 VP6 VP7 VP8	H6 (pin 5) H6 (pin 7) H6 (pin 9) H6 (pin 11) P6 (pin 5) P6 (pin 7) P6 (pin 9) P6 (pin 11)	F7 (pin 10) F7 (pin 8) F7 (pin 3) F7 (pin 11) N7 (pin 10) N7 (pin 8) N7 (pin 3) N7 (pin 11)	Vertical position data signals. These signals are applied to a coarse (N7) and fine (F7) vertical line comparator. When the vertical line comparator vertical synchronization inputs IV through 128V match the vertical position data signal, the coarse and fine vertical line comparator (F7, N7) outputs will all be a high logic level.
PIC1 PIC2 PIC3 PIC4	E6 (pin 5) E6 (pin 7) E6 (pin 9) E6 (pin 11)	E7 (pin 9) E7 (pin 11) E7 (pin 14) E7 (pin 1)	Picture height data signals. These signals determine the height of the data roadway pylon to be displayed. For example, if the pylon is only to be six vertical lines high, PIC data signal code will be 0111 (7). When VP1 through VP4 is equal to IV through 8V, the outputs of F7 will all be a high logic level. Beginning with the next vertical line, the outputs of F7 will begin counting down. When the "A" inputs of E7 reach the count of six, output A<B E7 (pin 7) will be a high logic level.
$\overline{256H}$	E4 (pin 2)	K5, J5 (pin 1)	Horizontal timing signal that represents the horizontal blanking period when it is a high logic level. During horizontal blanking, horizontal position signals (HP1 through HP8) are transferred to the outputs of multiplexers K5 and L5. During the horizontal scan time, horizontal timing signals (1H through 128H) are transferred to the outputs of multiplexers K5 and L5.
256H	J3 (pin 13)	N3 (pin 12)	Horizontal position address inputs to match RAM (M4) and object RAMs (H4, J4, K4, and L4) during horizontal blanking. If the horizontal blanking period is preceding a horizontal scan line on which a roadway pylon is to be displayed, R/$\overline{W}$ (pin 12 of match and object RAMs) will receive a low logic level from the output of the vertical line comparator (P8 pin 6). Therefore data is written into the match and object RAMs. The

SCHEMATIC SIGNAL	FROM	TO	
			data written into the match RAM is a low logic level for RAM address locations (output of N3 pin 9). The data written into the object RAMs is PA1 through PA4.
PA1 PA2 PA3 PA4	P5 (pin 4) P5 (pin 7) P5 (pin 9) P5 (pin 12)	L4 (pin 13) K4 (pin 13) J4 (pin 13) H4 (pin 13)	During horizontal blanking period, these signals are from horizontal timing signals 8H, 16H, 32H and 64H (inputs to multiplexer L2). These signals are the data input to the object RAMs L4, K4, J4, and H4.
V BLANK CLK* $\overline{\text{COMP B}}$ MATCH $\overline{\text{MATCH}}$	J7 (pin 10) N4 (pin 8) P8 (pin 3) N3 (pin 5) N3 (pin 6)	M4 (pin 3) N3 (pin 3) N3 (pin 1) N5 (pin 9) P8 (pin 5)	During a horizontal scan line that is going to display a roadway pylon, the match RAM and object RAMs are addressed by timing signals 1H through 128H. Therefore the address input changes at a rate of 1H 256 times during a horizontal scan line. When the address comes to a point where a low logic level has been stored in the match RAM, one 12 MHz (CLK*) pulse later, match latch N3 output pin 5 becomes a high logic level. This results in the inverse data output of the object RAMs through flip-flop N5.
OBJ0 OBJ1 OBJ2 OBJ3	N5 (pin 3) N5 (pin 6) N5 (pin 11) N5 (pin 14)	P5 (pin 2) P5 (pin 5) P5 (pin 11) P5 (pin 14)	Roadway object address signal. During the scan line, these signals address the Roadway character RAM M6 through multiplexer P5 if MATCH signal goes to a high logic level. The signals cause a data output from roadway picture RAM E6.
PIC5 PIC6 PIC7 PIC8 $\overline{\text{MATCH}}$ ROADWAY	M6 (pin 5) M6 (pin 7) M6 (pin 9) M6 (pin 11) N3 (pin 6) L8 (pin 6)	M5 (pin 15) M5 (pin 1) M5 (pin 10) M5 (pin 9) M5 (pin 11) K8 (pin 4)	Roadway picture signals PIC5 through PIC8 are applied directly to the inputs of shift register M5. Since $\overline{\text{MATCH}}$ is a low logic level, the PIC5 through PIC8 signals are immediately clocked out of shift register at a 6-MHz rate. This signal, called the ROADWAY signal, is fed directly to the video output.

PROM SIGNALS

BD0	H1, J1, K1, L1 (pin 14)	F3 (pins 2 & 4)	These signals make up the data bus from Program PROMs (C1, D1, E1, F1, H1, J1, K1, L1) to the Microprocessor (schematic sheet 3). This data bus is unidirectional (one direction only) and goes only from Program PROMs to the Microprocessor. These signals are an output of Program PROMs as a result of an address input to Program PROMs. Program PROMs are only addressed by the ten least significant bits of the address bus.
BD1	H1, J1, K1, L1 (pin 13)	E3 (pins 12 & 14)	
BD2	H1, J1, K1, L1 (pin 12)	E3 (pins 2 & 4)	
BD3	H1, J1, K1, L1 (pin 11)	F3 (pins 5 & 7)	
BD4	C1, D1, E1, F1 (pin 14)	F3 (pins 12 & 14)	
BD5	C1, D1, E1, F1 (pin 13)	E3 (pins 9 & 11)	

SCHEMATIC SIGNAL	FROM	TO	SIGNAL DESCRIPTION
BD6	C1, D1, E1, F1 (pin 12)	E3 (pins 5 & 7)	
BD7	C1, D1, E1, F1	F3 (pins 9 & 11)	
BA0	C2 (pin 3)	C1, D1, E1, F1, H1, J1, K1, L1 (pin 5)	These signals are the ten least significant bits of the address bus from the Microprocessor. An address input to Program Memory will result in a data output. The individual PROM integrated circuit pairs selected are determined by the enabling signal. All PROM chips are not used at the same time.
BA1	C2 (pin 5)	C1, D1, E1, F1, H1, J1, K1, L1 (pin 6)	
BA2	C2 (pin 7)	C1, D1, E1, F1, H1, J1, K1, L1 (pin 7)	
BA3	C2 (pin 9)	C1, D1, E1, F1, H1, J1, K1, L1 (pin 4)	
BA4	C2 (pin 11)	C1, D1, E1, F1, H1, J1, K1, L1 (pin 3)	
BA5	C2 (pin 13)	C1, D1, E1, F1, H1, J1, K1, L1 (pin 2)	
BA6	B2 (pin 3)	C1, D1, E1, F1, H1, J1, K1, L1 (pin 1)	
BA7	B2 (pin 5)	C1, D1, E1, F1, H1, J1, K1, L1 (pin 17)	
BA8	B2 (pin 7)	C1, D1, E1, F1, H1, J1, K1, L1 (pin 16)	
BA9	B3 (pin 9)	C1, D1, E1, F1, H1, J1, K1, L1 (pin 15)	
$\overline{\text{PROM 0}}$	H2 (pin 5)	C1, H1 (pin 8)	These are the ROM enabling signals. With a low logic level signal the individual pairs of ROMs are enabled. The term PROM is an abbreviation for programmable read-only memory. The PROMs are programmed by Atari specifically for the Night Driver game. These PROMs have the capability of being programmed only once. Therefore, for all practical purposes these eight chips may be referred to as ROMs.
$\overline{\text{PROM 1}}$	H2 (pin 6)	D1, J1 (pin 8)	
$\overline{\text{PROM 2}}$	H2 (pin 7)	E1, K1 (pin 8)	
$\overline{\text{PROM 3}}$	H2 (pin 9)	F1, L1 (pin 8)	

PAGE ZERO SIGNALS

SCHEMATIC SIGNAL	FROM	TO	SIGNAL DESCRIPTION
BA0 BA1 BA2 BA3 BA4 BA5 BA6 BA7	C2 (pin 3) C2 (pin 5) C2 (pin 7) C2 (pin 9) C2 (pin 11) C2 (pin 13) B2 (pin 3) B2 (pin 5)	A1, B1 (pin 4) A1, B1 (pin 3) A1, B1 (pin 2) A1, B1 (pin 1) A1, B1 (pin 17) A1, B1 (pin 5) A1, B1 (pin 6) A1, B1 (pin 7)	These are the address bus signals to the Page Zero (Scratch Pad) Memory. With an address code input to Page Zero Memory, the Microprocessor writes a data code into the Memory. At this time it is necessary for the read/write ($R/\overline{W}$) input (A1, B1 pin 16) to be a low logic level and output disable (OD) input (A1, B1 pin 9) to be a high logic level. The data recorded into the Page Zero Memory can later be read by the Microprocessor if the $R/\overline{W}$ input is a high logic level and OD is a low logic level. An address input will then cause the output of data that was previously stored at that address location.
SCHEMATIC SIGNAL	**From/To**	**From/To**	**SIGNAL DESCRIPTION**
BD0 BD1 BD2 BD3 BD4 BD5 BD6 BD7	F3 (pins 2 & 4) E3 (pins 12 & 14) E3 (pins 2 & 4) F3 (pins 5 & 7) F3 (pins 12 & 14) E3 (pins 9 & 11) E3 (pins 5 & 7) F3 (pins 9 & 11)	A1 (pin 11) A1 (pin 12) A1 (pin 13) A1 (pin 14) B1 (pin 11) B1 (pin 12) B1 (pin 13) B1 (pin 14)	These are bi-directional data lines from the Microprocessor to the Page Zero Memory or to the Microprocessor from the Page Zero Memory. The determining factor as to the direction of the data signal is the $R/\overline{W}$ signal and the OD (A1, B1 pin 9) signal. If the data signal is *to* the Page Zero Memory, OD must be a high logic level. If the data signal is *from* Page Zero Memory, OD must be a low logic level.
SCHEMATIC SIGNAL	**FROM**	**TO**	**SIGNAL DESCRIPTION**
$BR/\overline{W}$	B4 (pin 13)	E4 (pin 3)	Read/write bus. This signal is a high logic level when data is read *from* the Page Zero Memory and a low logic level when data is written *into* Page Zero Memory.
$B\Phi 2$	E4 (pin 6)	F4 (pin 5)	Phase 2 bus. This is a timing signal from the Microprocessor. When $B\Phi 2$ is a high logic level, data is manipulated to and from the Microprocessor. Refer to Section IV, subpapragraph 4.3.3.
$\overline{SCRAM}$	J2 (pin 1)	A1, B1 (pin 15)	Scratch Pad RAM (Page Zero Memory) enable. This signal originates in the Enable (Address Decoder) J2. This signal must be a low logic level before Page Zero Memory will operate.

IX. SCHEMATICS, DRAWINGS, AND PARTS LIST

NUMBER	TITLE
A006264-01	Parts List and Drawing Final Assembly
A006262-01	Parts List and Drawing Dashboard Assembly
A006547-01	Drawing Electronic Tray Assembly
A006321-01	Parts List, Drawing, and Schematic Night Driver PCB
A000607	Parts List, Drawing, and Schematic Steering Board PCB
006543-01	Schematic Harness
(none)	Schematic Motorola Model XM701-10 TV Monitor

NIGHT DRIVER

ASSEMBLY TITLE	FINAL ASSEMBLY	P/L A006264-01

PARTS LIST SPECIFICATION — Page 1 of 2

Drawn Barney Huang		
Checked	Mech. Eng.	
Proj. Eng.	Elec. Eng.	Rev.
	Mfg. Eng.	D

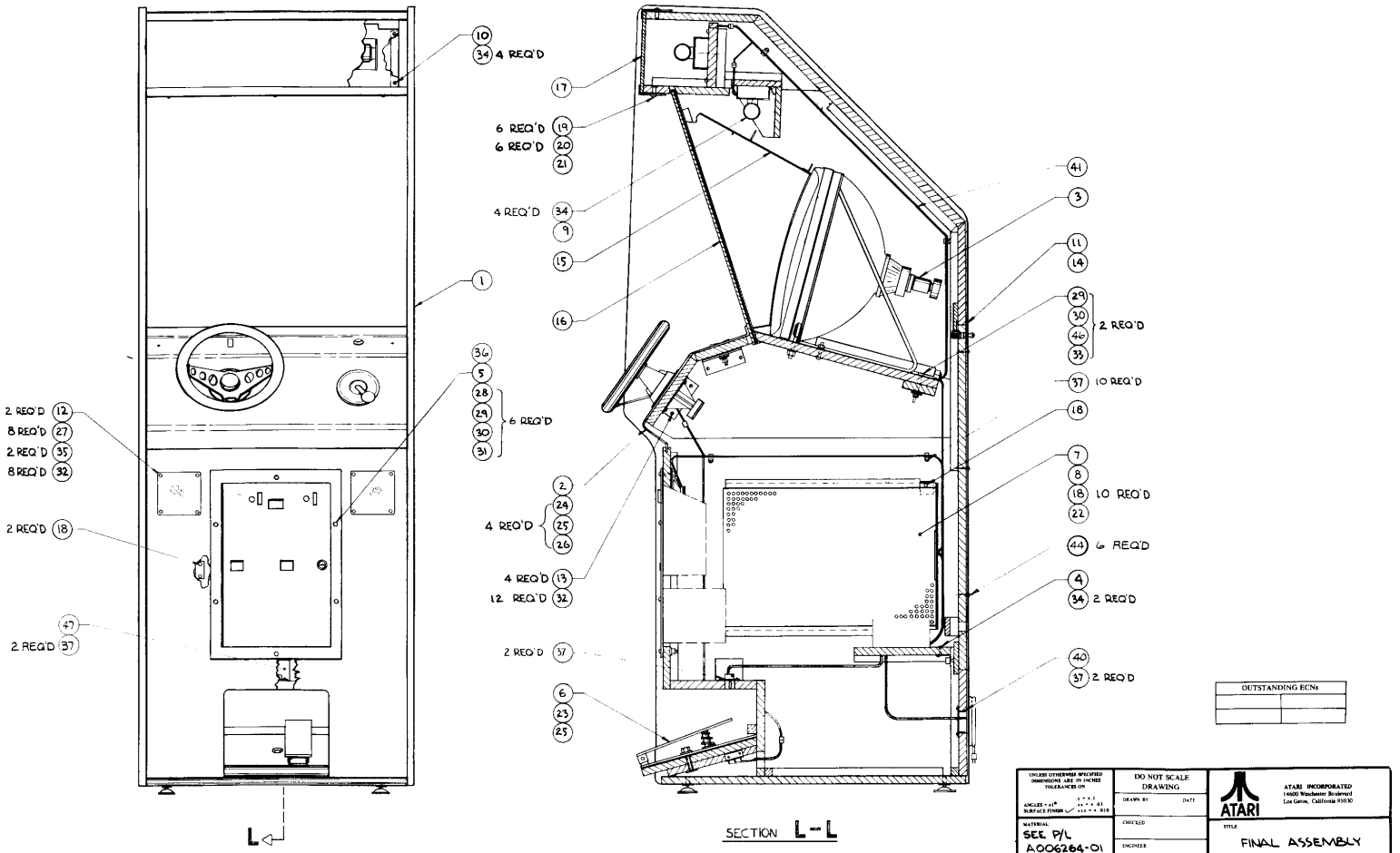
Rev.	Description	Date	Apprv.	Rev.	Description	Date	Apprv.
A	[illegible]	9/30/76					
B	Rev per ECN 3073	10/5/76					
C	Rev per ECN 3098	10/13/76					
D	Rev per ECN 3110	10/15/76					

Item	Part Number	Qty.	Description
1	A006234-02	1	Cabinet Assembly with Graphics
2	A006262-01	1	Dashboard Assembly
3	A006263-01	1	T.V. Shelf Assembly
4	A006547-01	1	Electronic Tray Assembly
5	A003637-11	1	Coin Door Assembly
6	A006315-01	1	Single Foot Pedal Assembly
7	A005912-01	1	R.F. Shield Box Assembly
8	A006690-01	1	R.F. Board Assy (N.Driver)
9	A006237-01	1	Black-Lite Display Assy
10	A006245-01	1	Display Assembly
11	A005906-01	1	Rear Door Assy
12	000869-01	2	Speaker Grill
13	002728-01	4	Bracket, Panel Mtg.
14	005233-01	A/R	Rear Door Seal
15	A006572-01	1	Bezel, 23" Monitor (Silkscreened)
16	006251-02	1	Plex, Main Display
17	006571-01	1	Plex, Attraction Panel (Silkscreen)
17A	005843-01	Ref	Plex, Light Box Panel
18	72-6608	13	Screw, Sm. Pan Hd., #6 x .50" Lg.
19	75-99090006	6	Well Nut, Blind Hole Fastener
20	82-8016	6	Screw, Button Hd., Socket 10-32 x 1.00" Lg.
21	003053-01	2	Plex Retainers
22	A006321-01	1	P.C. Board Assy
23	72-5524	1	Screw, Mach, Hex. Hd., Stl ¼-20 x 1.50" Lg.
24	75-015S	4	Washer, Flat ¼
25	75-045	5	Washer, Split Lock ¼
26	75-915S	4	Nut, Mach, Hex, ¼-20
27	73-77002	8	Pop Rivet, 3/16 O.D. x 3/4" Lg.
28	75-5124B	6	Carriage Bolt, 10-24 x 1.50" Lg.
29	75-040	8	Washer, Split-Lock #10
30	75-911S	8	Nut, Hex, Hd., #10-24
31	75-010S	8	Washer, Flat #10
32	72-6812	20	Screw, Sm., Pan Hd., Phil., #8 x 3/4 Lg.
33	75-5132N	2	Carriage Bolt, 10-24 x 2.00" Lg.
34	72-6820	10	Screw, Sm., Pan Hd., Phil., #8 x 1.25 Lg.
35	48-004	2	4" Speaker
36	75-931	1	10-24 Wing Nut
37	72-6610	14	Screw, Sm., Pan Hd., Phil., #6 x 5/8" Lg.
38	006319-01	1	Copy Right Decal
39	A006266-01	1	Shipping Container

ASSEMBLY TITLE FINAL ASSEMBLY P/L A006264-01 REV. 1

PARTS LIST SPECIFICATION Page 2 of 2

Item	Part Number	Qty.	Description
40	78-25001	1	Screw Down Tie Wrap
41	A006544-01	1	Main Harness
42	006543-01	1	Harness Schematic
43	TM-080	1	Tech Manual
44	006305-01	1	Poly Bay
45	82-1824	6	Wood Screws, #8 x 1.25" Lg. Flat Hd. Phil.



OUTSTANDING ECNs	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON ANGLES ± SURFACE FINISH	DO NOT SCALE DRAWING DRAWN BY DATE CHECKED ENGINEER PROJECT ENGINEER MFG ENGINEER	ATARI INCORPORATED 14600 Winchester Boulevard Los Gatos, California 95030
MATERIAL SEE P/L A006264-01		TITLE FINAL ASSEMBLY
FINISH		SIZE D · DRAWING NO A006264-01 · REV E SCALE · SHEET 1 OF 1

NIGHT DRIVER

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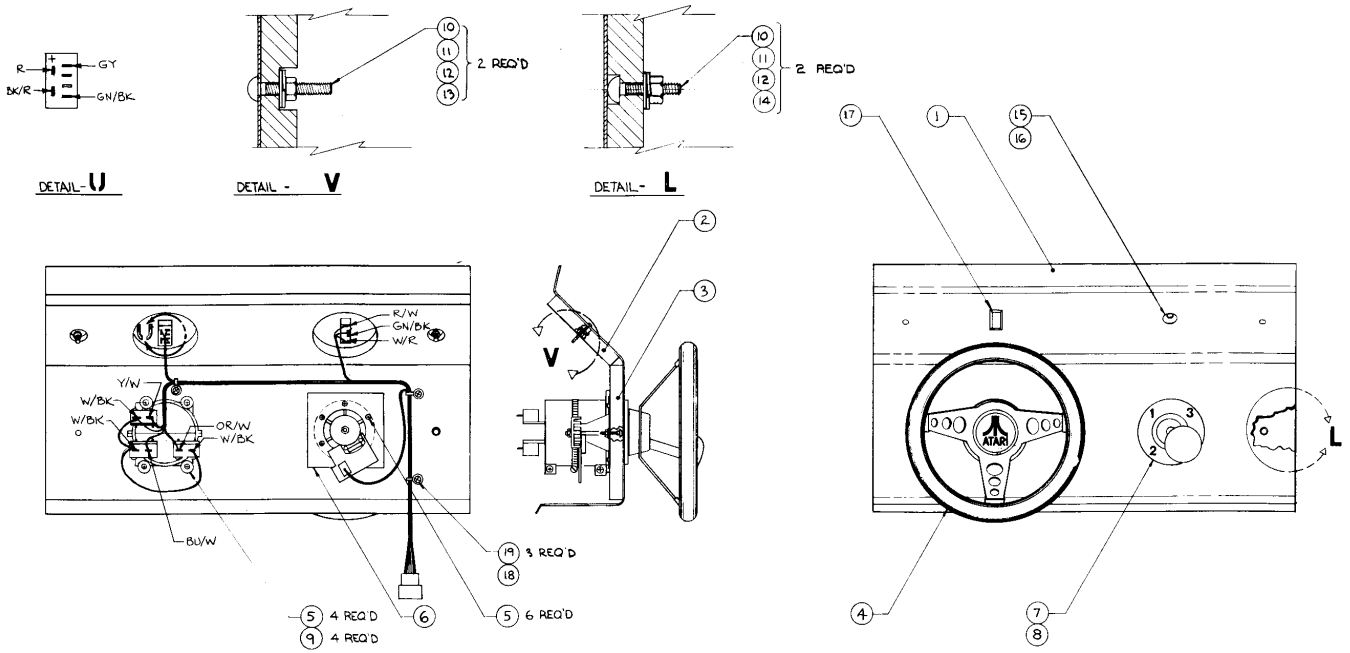
ASSEMBLY TITLE / DASHBOARD ASSY	P/L A006262-01

PARTS LIST SPECIFICATION Page 1 of 1

Drawn			
Checked		Mech. Eng.	
Proj. Eng.		Elec. Eng.	Rev.
		Mfg. Eng.	C

Rev.	Description	Date	Apprv.	Rev.	Description	Date	Apprv.
A	PROD REL	9/30/76					
B	Rev per ECN 3096	10/12/76					
C	Rev per ECN 3131	10/22/76					

Item	Part Number	Qty.	Description
1	006261-01	1	Control Panel with Graphics
2	006248-01	1	Control Panel (Top-Wood)
3	006249-01	1	Control Panel (Main-Wood)
4	000598-03	1	Steering Wheel Assy, (10" Dia Wheel)
5	85-22F112	10	Screw, Mach., Pan Hd., Phil., #10-24, 3/4 Lg. Type F.
6	000567	1	Bow Washer
7	A000608-02	1	N-Shift Assembly
8	005255-01	1	Shift Bezel
9	75-010S	4	#10 Flat Washer
10	75-015S	4	#¼-20 Flat Washer
11	75-045	4	#¼-20 Lock Washer
12	75-915S	4	#¼-20 Hex Nut
13	75-5524B	2	#¼-20 x 1.50" Lg. Carriage Bolts
14	75-5524N	2	#¼-20 x 1.50" Lg. Carriage Bolts
15	62-002	1	Led Switch
16	001856-01	1	Aluminum Bushing, Switch
17	61-081C	1	Rocker Switch Snap in Bezel (Gold Contacts, Dry Circuit)
18	A006546-01	1	Control Panel Harness
19	72-6610	3	Screw, Sm., Pan HD., Phil., #6 x 5/8 "Lg.



OUTSTANDING ECNs	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: ANGLES ± 1° .X ± .1 .XX ± .03 .XXX ± .010 SURFACE FINISH	DO NOT SCALE DRAWING DRAWN BY DATE CHECKED ENGINEER PROJECT ENGINEER MFG ENGINEER	ATARI INCORPORATED 1400 Wrecker Boulevard Los Gatos, California 95030
MATERIAL: SEE P/L A006262-01		TITLE: DASHBOARD ASSEMBLY
FINISH		SIZE D · DRAWING NO A006262-01 · REV C SCALE · SHEET 1 OF 1

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NIGHT DRIVER

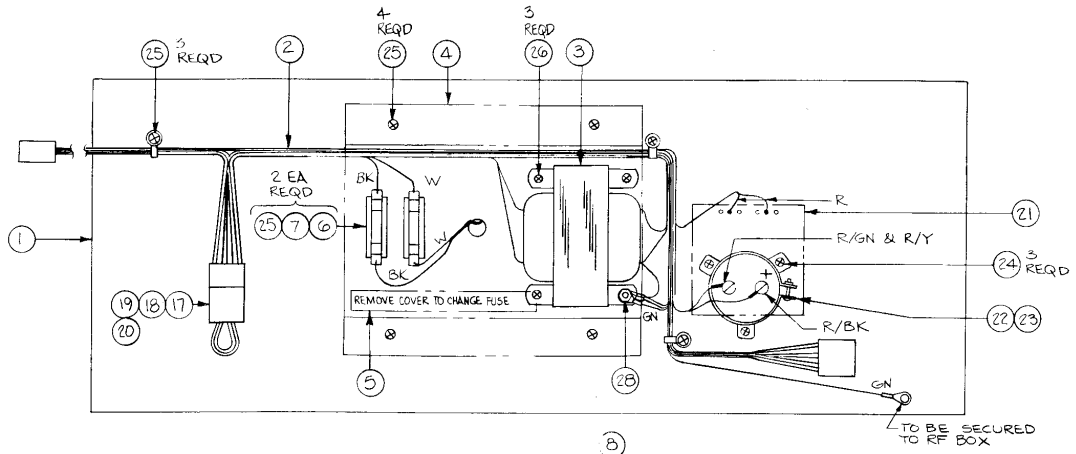
ASSEMBLY TITLE / ELECTRONICS TRAY ASSY	P/L A006547-01

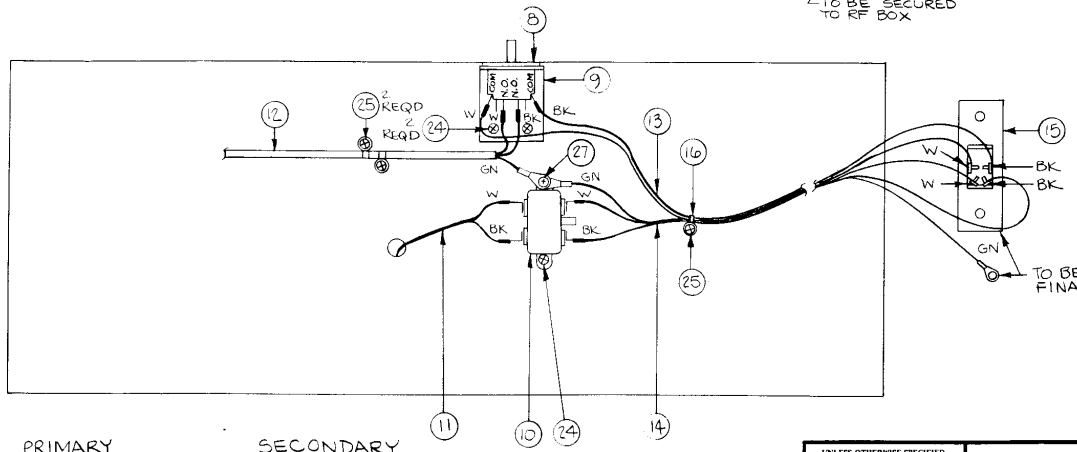
PARTS LIST SPECIFICATION Page 1 of 1

Drawn	NEXT ASSY A006264-01	
Checked	Mech. Eng.	
Proj. Eng.	Elec. Eng.	Rev. D
	Mfg. Eng.	

Rev.	Description	Date	Apprv.	Rev.	Description	Date	Apprv.
A		9/30/76					
B	Rev per ECN 3079	10/6/76					
C	Rev per ECN 3100	10/13/76					
D	Rev per ECN 3119						

Item	Part Number	Qty.	Description
1	006250-01	1	Electronics Tray
2	A006545-01	1	Power Supply Harness
3	001551-01 or -02	1	Transformer, 001551
4	000622-01	1	Cover, Transformer
5	000871-01	1	Label
6	46-201202	2	Fuse, 2 Amp
7	79-3202	2	Fuse Holder
8	68-002	1	Interlock Switch
9	000268-02	1	Bracket, Switch Mounting
10	41-2001	1	Filter, Power Line
11	A006550-01	1	Mini-Harness
12	A006222-01	1	Power Cord Assy, 8 Ft
13	A006447-01	1	Power in On-Off Switch Harness
14	A006448-01	1	Power Out On-Off Switch Harness
15	A006449-01	1	On-Off Switch Assy
16	78-25001	1	Screw Down Tie Wrap
17	A001921-01	A/R	Shorting Block, 95V
18	A001921-02	"	" " 110V
19	A001921-03	"	" " 220V H
20	A001921-04	"	" " 220V L
21	A006555-01	1	PC Board, Rectifier
22	29-053	1	Capacitor, Sprague Electrolytic 26,000 uf @15V
23	78-70501SC	1	Bracket, Capacitor Mounting Sprague #4586-48
24	72-6608	6	Screw, Sm, Pan Hd, Phil #6 x ½ Lg.
25	72-6612	8	" " " " " #6 x 3/4 Lg.
26	72-6812	7	" " " " " #8 x 3/4 Lg.
27	75-2820B	1	Screw, Mach., Rd Hd, Brass #8 - 32 x 1¼ Lg.
28	75-918B	1	Nut, Mach, Brass, #8-32





OUTSTANDING ECNs	

PRIMARY

OR	Y	BU	R	R
1	2	3	7	9
4	5	6	8	
GN	BK	V	R/Y	

SECONDARY

OR	GY	OR
12	11	10
15	14	13
GN	BU	BU

TRANSF WIRE COLORS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: ANGLES = ±1° SURFACE FINISH ✓ x = ±.1 xx = ±.03 xxx = ±.010	DO NOT SCALE DRAWING	ATARI INCORPORATED 14600 Winchester Boulevard Los Gatos, California 95030
MATERIAL: SEE P/L	DRAWN BY DATE	TITLE: NIGHT DRIVER ELECTRONICS TRAY ASSEMBLY
FINISH:	CHECKED	
	ENGINEER	
	PROJECT ENGINEER	
	MFG ENGINEER	SIZE C · DRAWING NO A006547-01 · REV D
		SCALE 1:2 · SHEET 1 OF 1

NIGHT DRIVER

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ASSEMBLY TITLE / Assy, Night Driver P.C.B. **P/L** A006321-01

PARTS LIST SPECIFICATION Page 1 of 4

Drawn H. Slade		
Checked	Mech. Eng.	
Proj. Eng.	Elec. Eng.	Rev.
	Mfg. Eng.	A

Rev.	Description	Date	Apprv.	Rev.	Description	Date	Apprv.
A	PROD REL.						

Item	Part Number	Qty.	Description
1	006322-01	1	Printed Circuit Board
2	10-5470	1	Resistor, Carbon Comp, 1/4w, 5%, 47 ohm R83
3	10-5101	2	Resistor, Carbon Comp, 1/4w, 5%, 100 ohm R16, 42
4	10-5151	1	Resistor, Carbon Comp, 1/4w, 5%, 150 ohm R51
5	10-5221	3	Resistor, Carbon Comp, 1/4w, 5%, 220 ohm R49, 50, 68
6	10-5331	3	Resistor, Carbon Comp, 1/4w, 5%, 330 ohm R4, 5, 109
7	10-5471	26	Resistor, Carbon Comp, 1/4w, 5%, 470 ohm R19, 20, 22, 25, 70-73, 75-82, 94-98, 101-104, 113
8			
9	10-5102	30	Resistor, Carbon Comp, 1/4w, 5%, 1K ohm R1, 2, 7, 18, 21, 23, 24, 26-41, 48, 52, 53, 67, 69, 89, 112
10	10-5222	8	Resistor, Carbon Comp, 1/4w, 5%, 2.2K ohm R54, 63-66, 99, 105, 106
11	10-5332	1	Resistor, Carbon Comp, 1/4w, 5%, 3.3K ohm R45
12	10-5392	2	Resistor, Carbon Comp, 1/4w, 5%, 3.9K ohm R56, 100
13	10-5472	1	Resistor, Carbon Comp, 1/4w, 5%, 4.7K ohm R62
14	10-5682	2	Resistor, Carbon Comp, 1/4w, 5%, 6.8K ohm R15, 61
15	10-5822	2	Resistor, Carbon Comp, 1/4w, 5%, 8.2K ohm R46, 55
16	10-5912	1	Resistor, Carbon Comp, 1/4w, 5%, 9.1K ohm R43
17	10-5103	2	Resistor, Carbon Comp, 1/4w, 5%, 10K ohm R44, 60
19	10-5183	1	Resistor, Carbon Comp, 1/4w, 5%, 18K ohm R17
20	10-5271	1	Resistor, Carbon Comp, 1/4w, 5%, 270 ohm R108
21	10-5473	3	Resistor, Carbon Comp, 1/4w, 5%, 47K ohm R47, 58, 59
22	10-5104	2	Resistor, Carbon Comp, 1/4w, 5%, 100K ohm R12, 90
23	10-5224	2	Resistor, Carbon Comp, 1/4w, 5%, 220K ohm R8, 13
24	10-5474	1	Resistor, Carbon Comp, 1/4w, 5%, 470K ohm R9
25	10-5105	1	Resistor, Carbon Comp, 1/4w, 5%, 1Megohm R10
26	10-5225	1	Resistor, Carbon Comp, 1/4w, 5%, 2.2Megohm R11
27	10-5681	1	Resistor, Carbon Comp, 1/4w, 5%, 680 ohm R6

Item	Part Number	Qty.	Description
28	10-5184	1	Resistor, Carbon Comp, 1/4w, 5%, 180K ohm R110
29	12-5151	1	Resistor, Carbon Comp, 1w, 5%, 150 ohm R57
30	19-8D9W2P0	1	Resistor, Wirewound, 20w, 2 ohm R74
31	19-315502	1	Potentiometer, 5K R111
32	19-315504	1	Potentiometer, 100K R14
34	27-250102	4	Capacitor, Ceramic Disc, 25V, .001uf C5, 7, 9, 23
35	27-250103	2	Capacitor, Ceramic Disc, 25V, .01uf C18, 24
36	27-250104	29	Capacitor, Ceramic Disc, 25V, .1uf C1, 19, 20, 22, 25, 26, 28-50
37	27-250304	1	Capacitor, Ceramic Disc, 25V, .33uf C12
39	21-101224	2	Capacitor, Mylar, 100V, .22uf C6, 11
40	28-101221	1	Capacitor, Dipped Mica, 100V, 220pf C21
43	29-006	1	Capacitor, Tantalum, 35V, 1uf C4
45	24-250105	1	Capacitor, Electrolytic, 25V, 1uf C17
46	24-250225	3	Capacitor, Electrolytic, 25V, 2.2uf C3, 15, 16
47	24-250106	1	Capacitor, Electrolytic, 25V, 10uf C10
48	24-250226	1	Capacitor, Electrolytic, 25V, 22uf C13
50	24-250476	1	Capacitor, Electrolytic, 25V, 47uf C8
51	24-250227	1	Capacitor, Electrolytic, 25V, 220uf C2
52	24-250108	1	Capacitor, Electrolytic, 25V, 1000uf C14
53	24-250478	1	Capacitor, Electrolytic, 25V, 4700uf C27
56	31-1N914	3	Diode 1N914 CR1, 2, 3
57	32-1N962B	1	Diode, Zener, 1N962B CR4
58	38-MV5013	3	LED, Red, MV5013 CR5, 6, 7
60	34-2N3643	2	Transistor 2N3643 Q2, 3
62	37-7400	3	I.C. 7400 H3, F4, C7
63	37-7402	1	I.C. 7402 C4
64	37-7404	3	I.C. 7404 E4, N4, L8
66	37-7408	2	I.C. 7408 B8, P8
67	37-7410	1	I.C. 7410 D4
68	37-7414	2	I.C. 7414 J8, E9
69	37-7430	3	I.C. 7430 J5, P7, N8
70	37-7432	1	I.C. 7432 K8
71	37-7442	3	I.C. 7442 A2, H2, J2
72	37-7474	4	I.C. 7474 N3, H5, L7, E8
73	37-7483	2	I.C. 7483 F7, N3
74	37-7485	1	I.C. 7485 E7
75	37-7486	1	I.C. 7486 C6
76	37-7492	1	I.C. 7492 M3
77	37-74107	1	I.C. 74107 D8
78	37-74151	1	I.C. 74151 F9
79	37-74153	2	I.C. 74153 K9, M9
80	37-74S157	5	I.C. 74S157 or 93S22 K2, L2, K5, L5, P5
82	37-74164	2	I.C. 74164 D6, D7
83	37-74166	1	I.C. 74166 P3

ASSEMBLY TITLE Assy, Night Driver P.C.B. P/L A006321-01 REV. A

PARTS LIST SPECIFICATION

Item	Part Number	Qty.	Description	
84	37-74174	2	I.C. 74174	D5, E5
85	37-74175	1	I.C. 74175	J7
86	37-74S175	1	I.C. 74S175	N5
87	37-74191	1	I.C. 74191	M5
88	37-74193	1	I.C. 74193	C8
89	37-9316	5	I.C. 9316	J3, K3, L3, F8, H8
90	37-9321	1	I.C. 9321	K7
91	37-555	1	I.C. 555	C9
92	37-566	3	I.C. 566	A5, A6, A7
93	37-MFC6040	1	I.C. MFC6040	B7
94	37-MFC3040	1	I.C. MFC3040	B6
95	37-LM324	1	I.C. LM324	B5
96	37-8T97	5	I.C. 8T97 or 74367	M8, M1, B2, C2, B4
97	37-8T28	2	I.C. 8T28	E3, F3
98	37-TDA1004	1	I.C., Audio Amp, TDA1004	A9
99	37-LM323	1	I.C., Regulator, LM323	
102	90-6010	1	I.C.	C3
103	90-7002	1	I.C.	M2
104	90-7005	6	RAM 82S25	E6, H6, J6, M6, P6, L6
105	90-7008	5	RAM 82S16	H4, J4, K4, M4, L4
106	90-7015	2	RAM 2111-A	A1, B1
108	006559-01	1	PROM, Sync	H7
109	006560-01	1	PROM 1	H1
110	006561-01	1	PROM 2	C1
111	006562-01	1	PROM 3	J1
112	006563-01	1	PROM 4	D1
113	006564-01	1	PROM 5	K1
114	006565-01	1	PROM 6	E1
115	006566-01	1	PROM 7	L1
116	006567-01	1	PROM 8	F1
117	006568-01	1	PROM, Alpha-Numeric	P2
** 118	006569-01	1	MASK ROM 1	D2
** 119	006570-01	1	MASK ROM 2	E2
122	90-102	1	Crystal, 12.096Mhz	Y1
123	66-014P2T	1	DIP Switch, Hexa-Decimal	L10
124	66-114P1T	1	DIP Switch, 4PST	M10
125	79-42540	1	Socket, 40-Pin	
126	78-06001	1	Heatsink, LM323	
127	78-16005	1	Sil-Pad	
128	78-06009	1	Heatsink, TDA1004	
129	78-13016	A/R	Cement, Heatsink	
132	006457-01	18	Buss Bar, 13-Post	
133	72-1608C	2	Screw, Machine, Pan Hd., Phillips, #6-32 x 1/2" CRES	
134	75-016S	2	Washer, Flat, #6	

ASSEMBLY TITLE Assy, Night Driver P.C.B. P/L A006321-01 REV. A

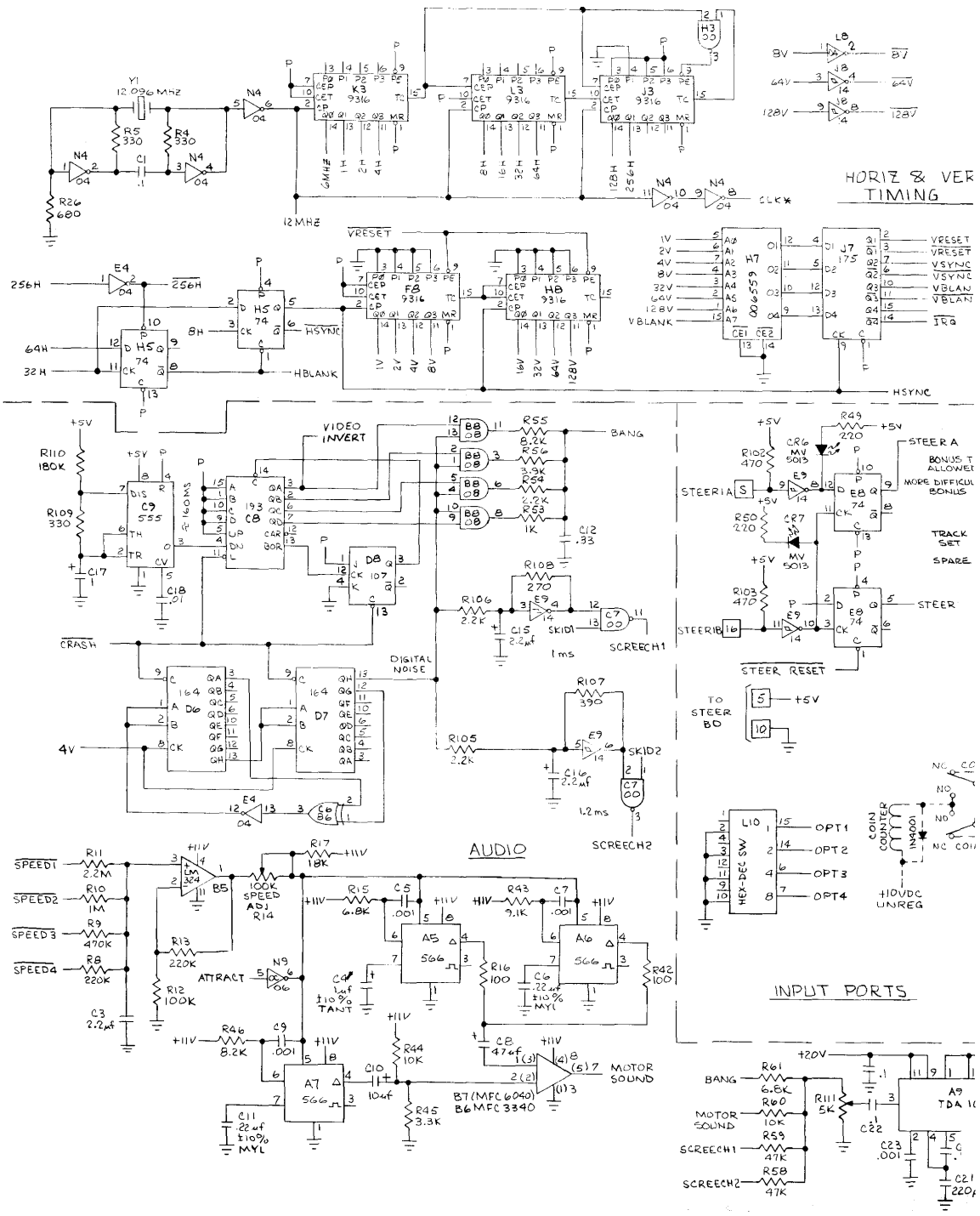
PARTS LIST SPECIFICATION

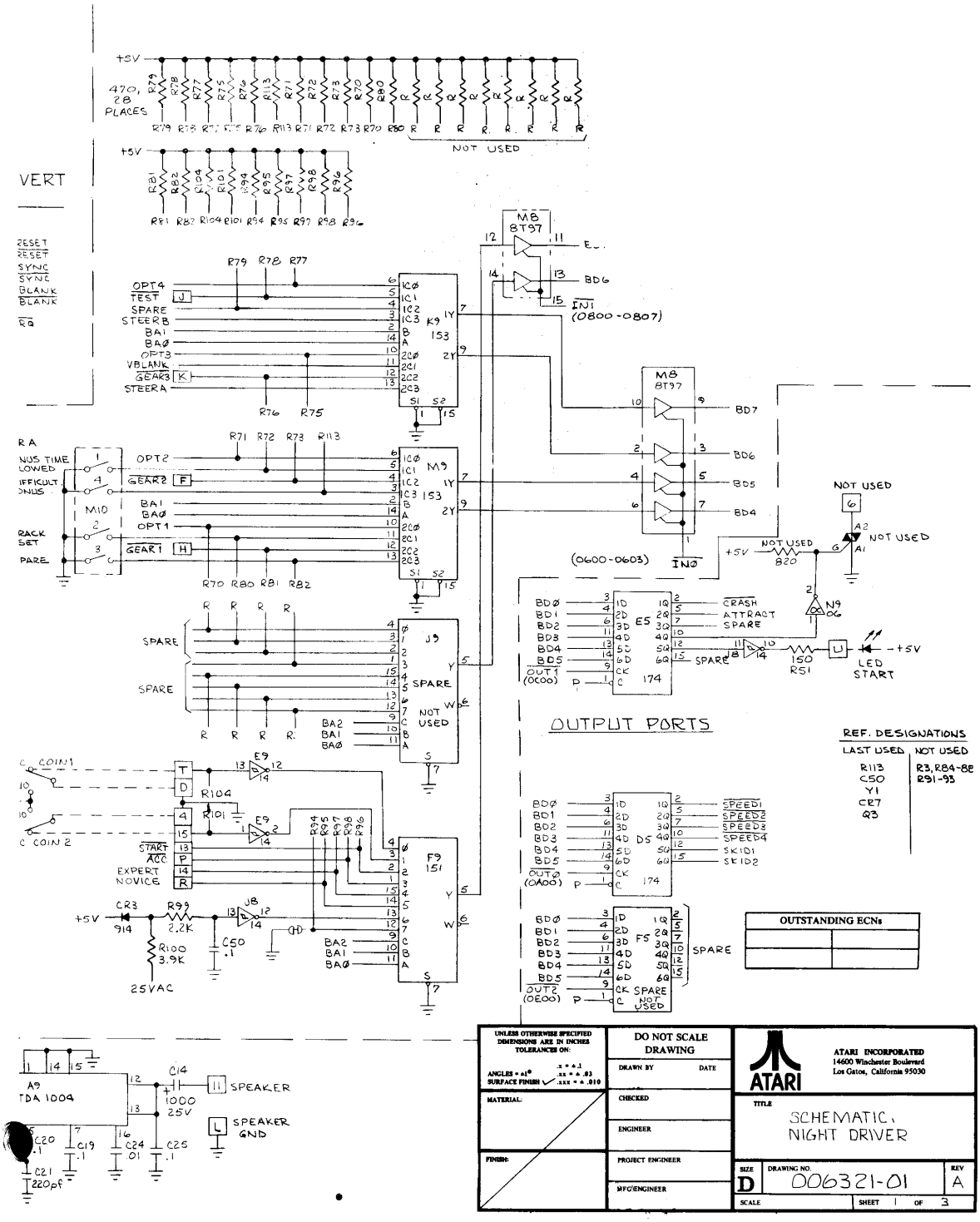
Item	Part Number	Qty.	Description	
135	75-056	2	Washer, Lock, Internal Star #6	
136	75-916C	2	Nut, Hex, #6-32, CRES	
137	10-5391	1	Resistor, Car. Comp, ¼W, 5%, 390 ohm	R107
138	31-A14F	2	Diode, A14F	CR8,9

NOTES:

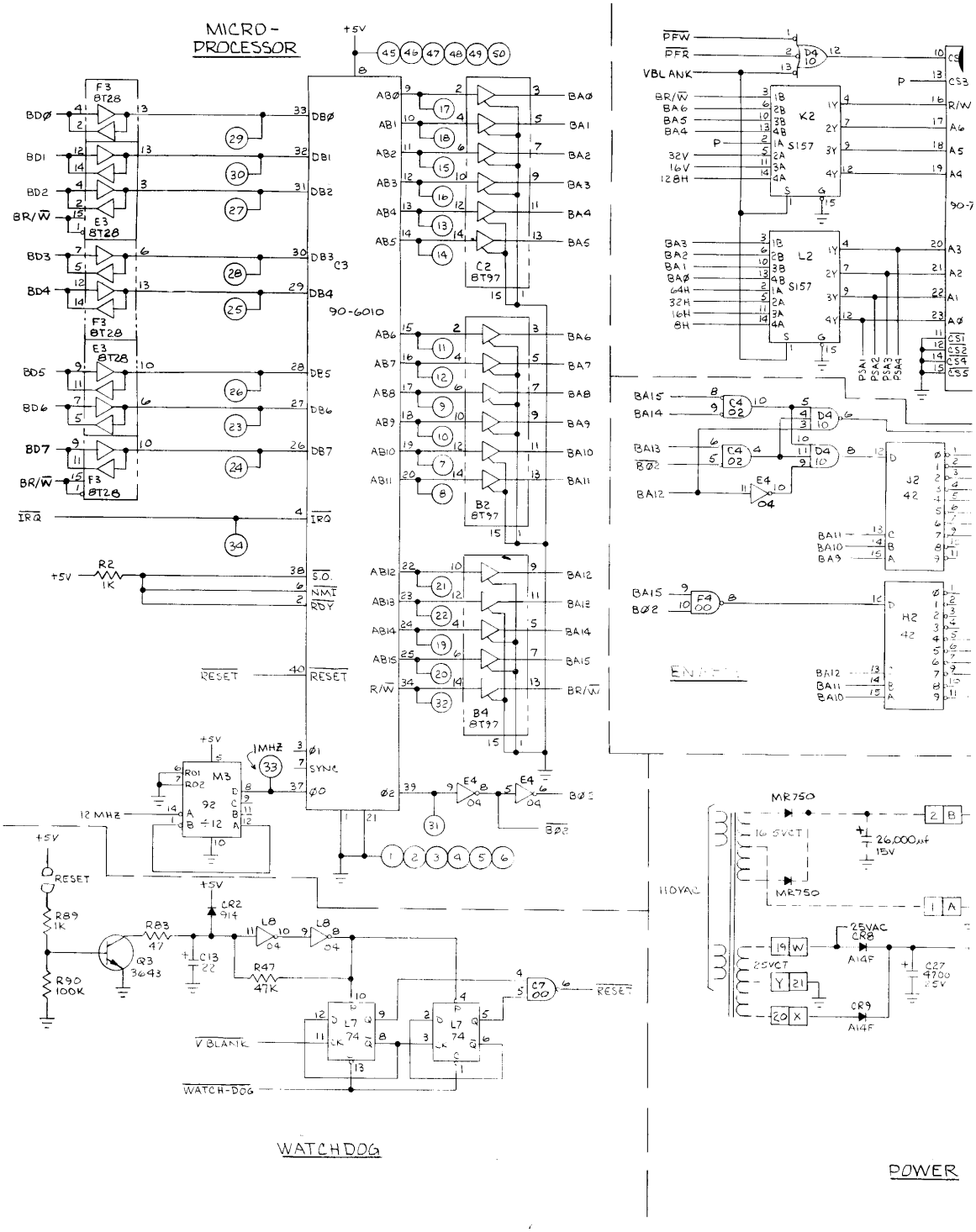
* MCF3040 To Replace MFC6040 When Stock is Depleted.

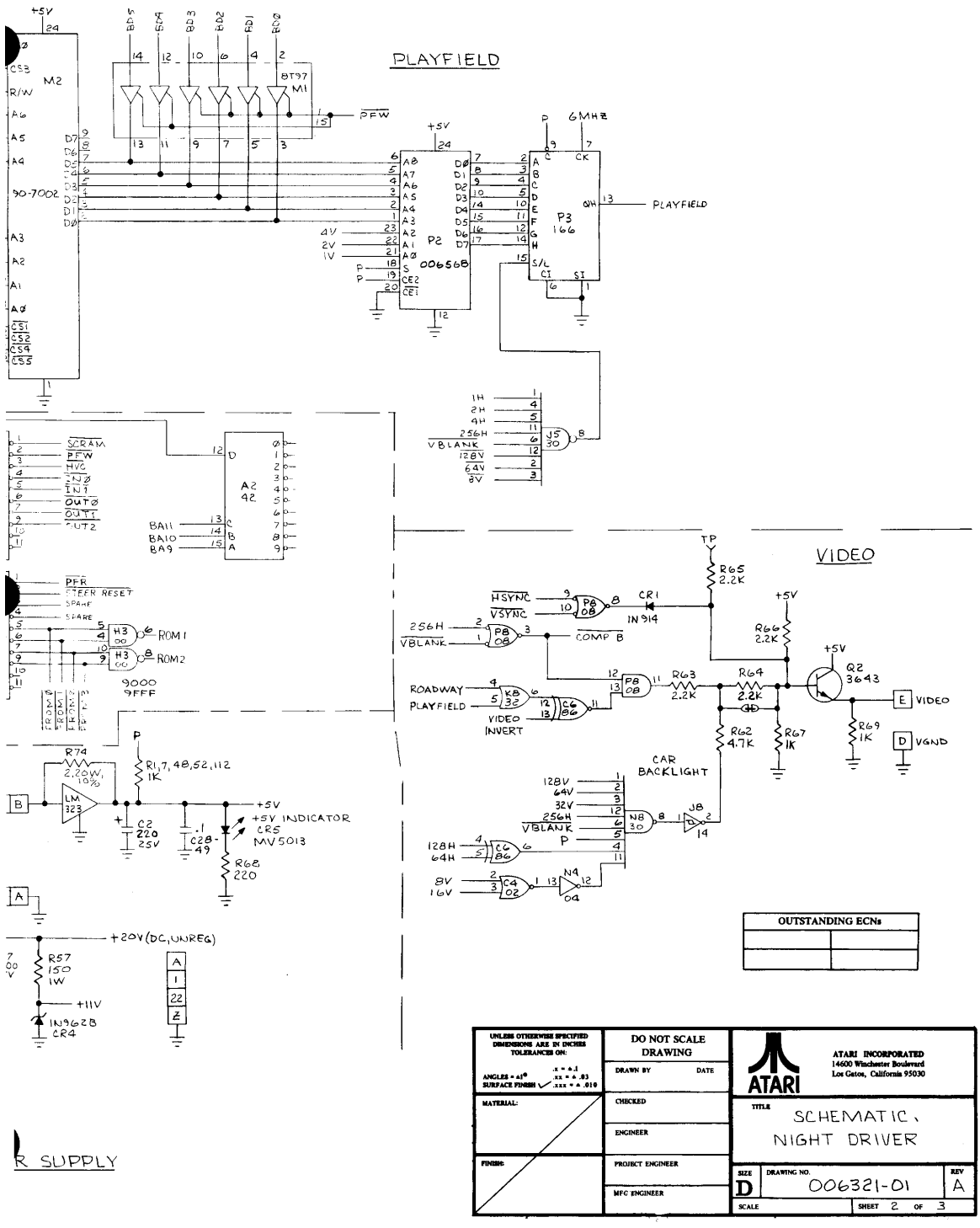
** Use Item 118, MASK ROM1, In Position D2
To Replace Items 109, 110, 111 & 112.
Use Item 119, MASK ROM 2, In Position F2
To Replace Items 113, 114, 115 & 116.


HORIZ & VER TIMING
AUDIO
INPUT PORTS
12 MHZ
VRESET
HSYNC
HBLANK
VIDEO INVERT
BANG
CRASH
DIGITAL NOISE
SCREECH1
SCREECH2
MOTOR SOUND
STEER A
STEER B
STEER RESET
TRACK SET
SPARE
BONUS T ALLOWE
MORE DIFFICUL BONUS
TO STEER BD
COIN COUNTER
+10VDC UNREG
SPEED1
SPEED2
SPEED3
SPEED4
ATTRACT
SPEED ADJ R14
OPT1
OPT2
OPT3
OPT4



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: ANGLES ± 1° SURFACE FINISH .x ± .1, .xx ± .03, .xxx ± .010	DO NOT SCALE DRAWING	ATARI INCORPORATED 14600 Winchester Boulevard Los Gatos, California 95030
MATERIAL:	DRAWN BY / DATE / CHECKED / ENGINEER / PROJECT ENGINEER / MFG/ENGINEER	TITLE: SCHEMATIC, NIGHT DRIVER
FINISH:		SIZE D · DRAWING NO. 006321-01 · REV A · SCALE · SHEET 1 OF 3

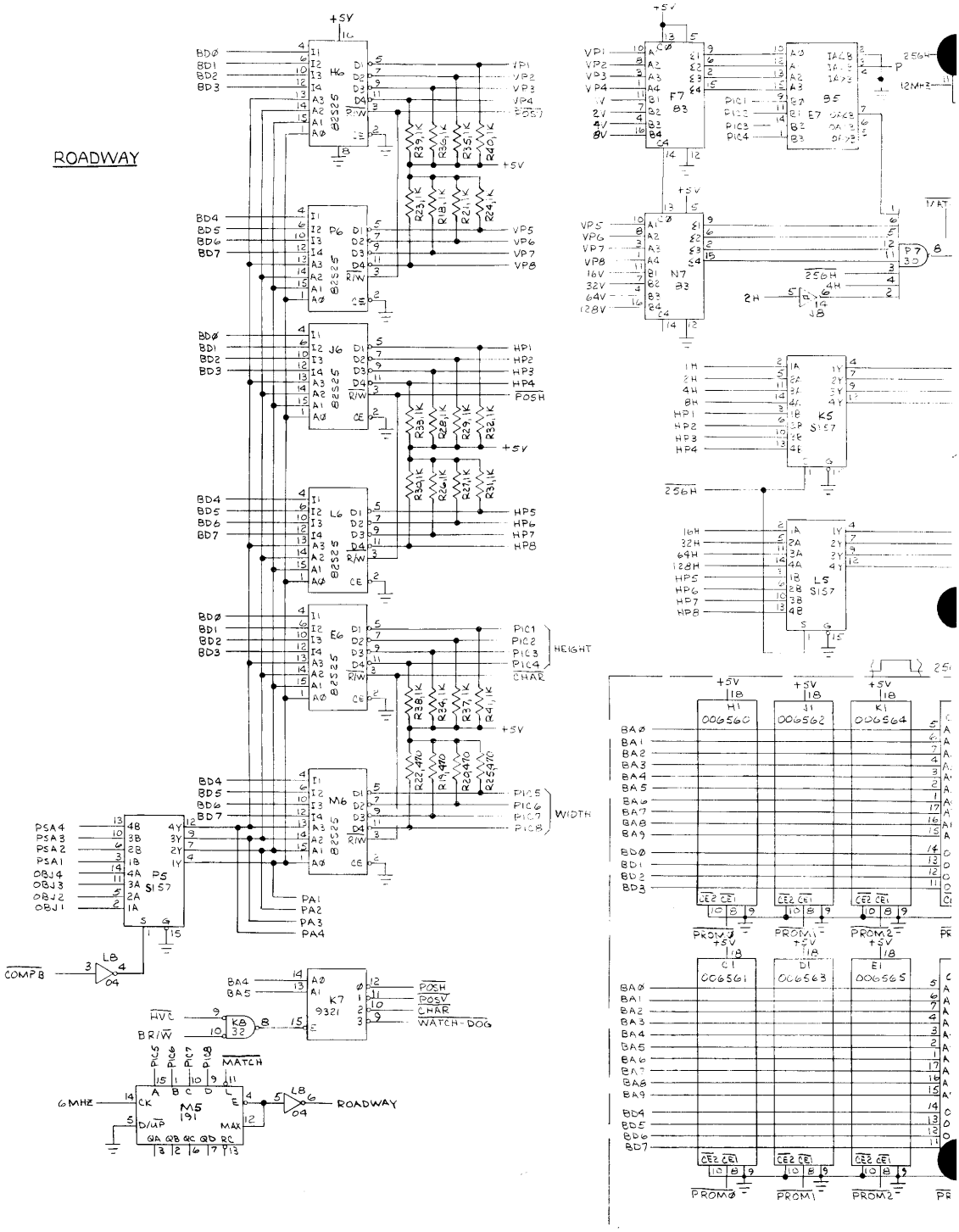

MICRO-
PROCESSOR
+5V
BD0
BD1
BD2
BR/W
BD3
BD4
BD5
BD6
BD7
IRQ
R2
1K
RESET
12 MHZ
1MHZ
R01
R02
M3
92
÷12
SYNC
R89
1K
R90
100K
Q3
3643
R83
47
CR2
914
C13
22
R47
47K
L8
04
L7
74
V BLANK
WATCH-DOG
WATCHDOG
PFW
PFR
VBLANK
BR/W
BA6
BA5
BA4
32V
16V
128H
K2
S157
L2
BA3
BA2
BA1
BA0
64H
32H
16H
8H
PSA1
PSA2
PSA3
PSA4
90-7
BA15
BA14
BA13
BA12
BA11
BA10
BA9
J2
42
H2
ENABLE
MR750
16 SVCT
26,000uf
15V
110VAC
25VAC
CR8
A14F
25VCT
C27
4700
25V
CR9
POWER

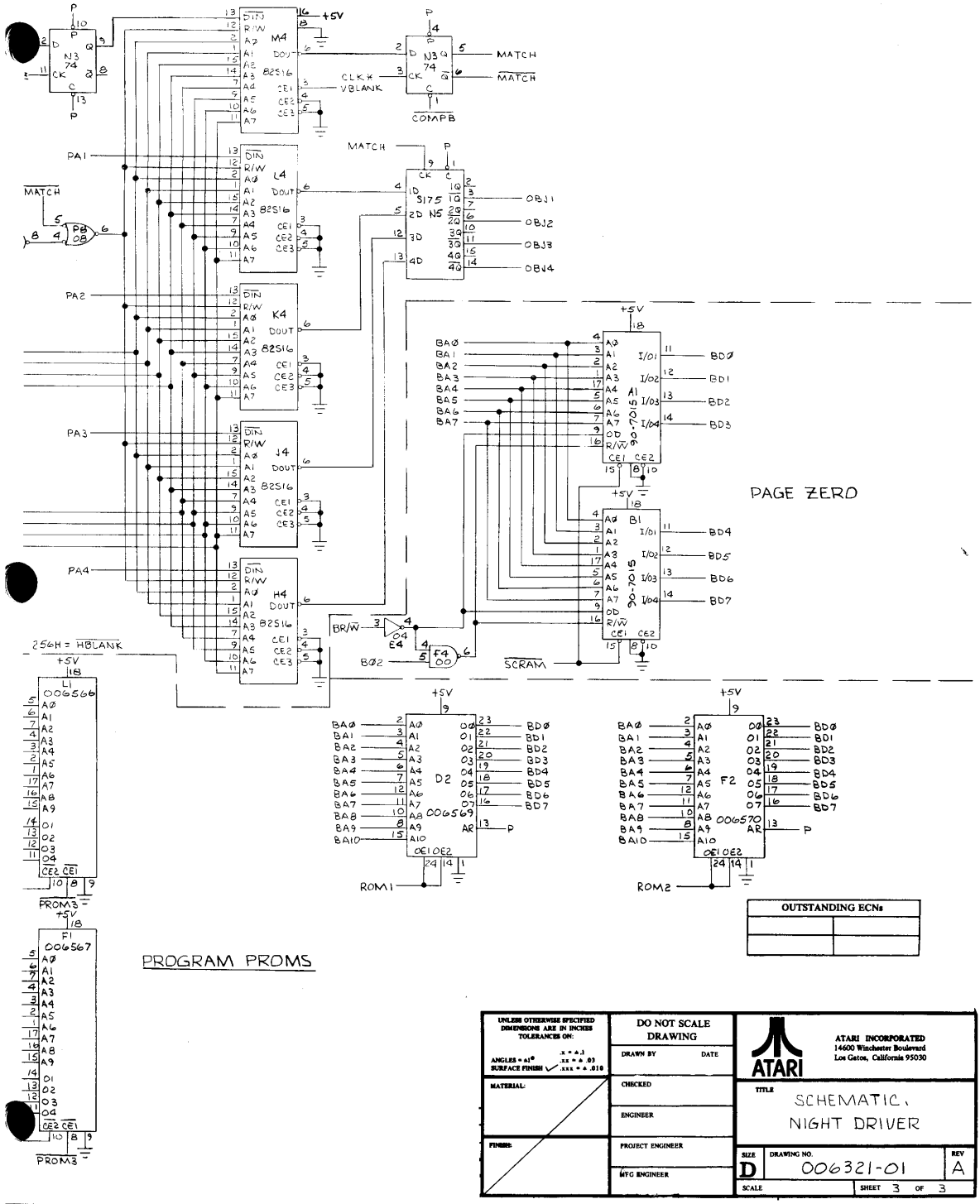


OUTSTANDING ECNs	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: ANGLES = ±1° SURFACE FINISH ✓ .x = ±.1 .xx = ±.03 .xxx = ±.010	DO NOT SCALE DRAWING	ATARI INCORPORATED 14600 Winchester Boulevard Los Gatos, California 95030
MATERIAL:	DRAWN BY / DATE	
	CHECKED	TITLE: SCHEMATIC, NIGHT DRIVER
	ENGINEER	
FINISH:	PROJECT ENGINEER	SIZE D · DRAWING NO. 006321-01 · REV A
	MFG ENGINEER	SCALE · SHEET 2 OF 3

ROADWAY


+5V
BD0
BD1
BD2
BD3
H6
82S25
VP1
VP2
VP3
VP4
POSV
R39,1K
R36,1K
R35,1K
R40,1K
BD4
BD5
BD6
BD7
J6
HP1
HP2
HP3
HP4
POSH
R33,1K
R28,1K
R29,1K
R32,1K
L6
HP5
HP6
HP7
HP8
R30,1K
R26,1K
R27,1K
R31,1K
E6
PIC1
PIC2
PIC3
PIC4
CHAR
HEIGHT
R38,1K
R24,1K
R37,1K
R41,1K
M6
PIC5
PIC6
PIC7
PIC8
WIDTH
R22,470
R19,470
R20,470
R25,470
PSA4
PSA3
PSA2
PSA1
OBJ4
OBJ3
OBJ2
OBJ1
P5
SI57
PA1
PA2
PA3
PA4
COMPB
LB
04
BA4
BA5
K7
9321
HVC
BR/W
KB
32
WATCH-DOG
MATCH
6MHZ
M5
191
D/UP
MAX
ROADWAY
F7
83
N7
83
VP5
VP6
VP7
VP8
16V
32V
64V
128V
256H
12MHZ
P
1/AT
P7
32
2H
4H
J8
K5
SI57
1H
2H
4H
8H
HP1
HP2
HP3
HP4
L5
SI57
16H
32H
64H
128H
HP5
HP6
HP7
HP8
H1
006560
J1
006562
K1
006564
BA0
BA1
BA2
BA3
BA4
BA5
BA6
BA7
BA8
BA9
BD0
BD1
BD2
BD3
PROM0
PROM1
PROM2
C1
006561
D1
006563
E1
006565
BD4
BD5
BD6
BD7



OUTSTANDING ECNs	

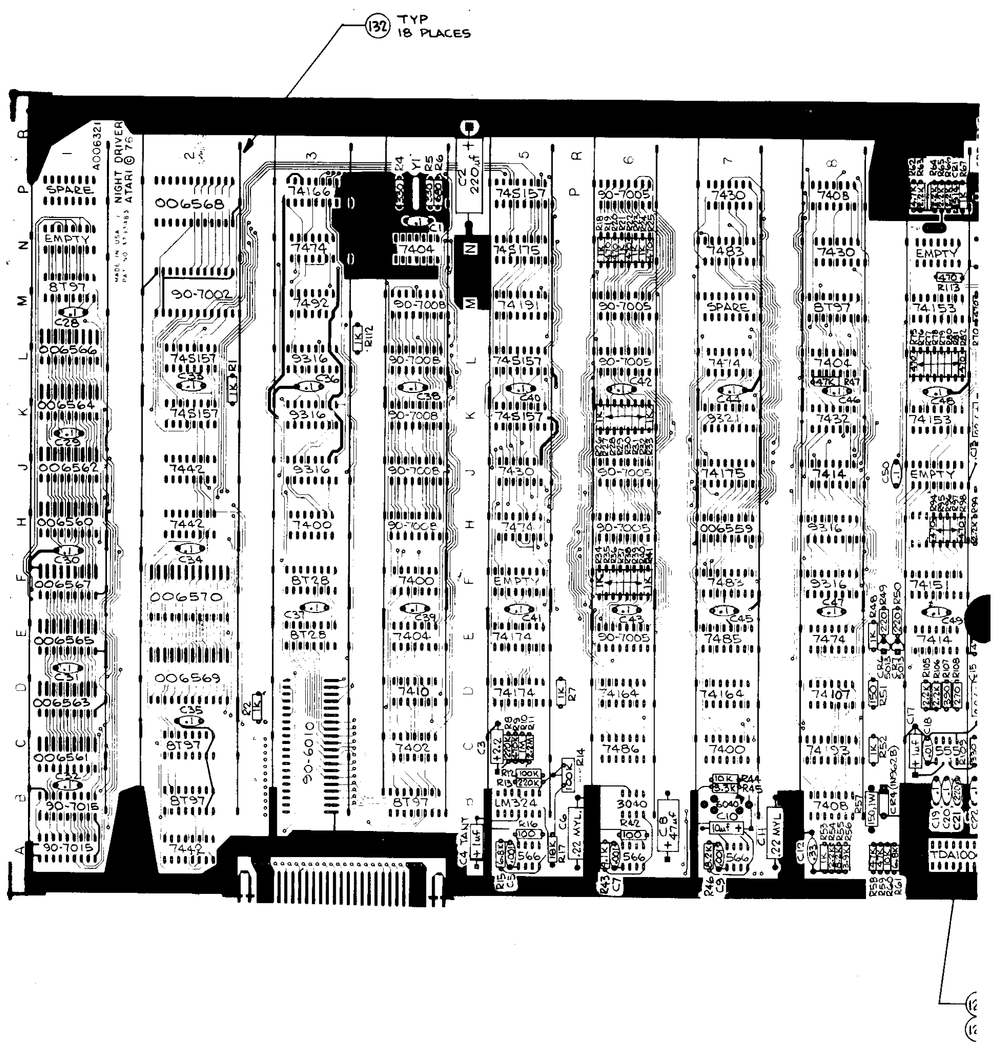
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: ANGLES = ±1° SURFACE FINISH	DO NOT SCALE DRAWING	ATARI INCORPORATED 14600 Winchester Boulevard Los Gatos, California 95030
MATERIAL:	DRAWN BY DATE	TITLE: SCHEMATIC, NIGHT DRIVER
FINISH:	CHECKED	
	ENGINEER	
	PROJECT ENGINEER	SIZE D — DRAWING NO. 006321-01 — REV A
	MFG ENGINEER	SCALE — SHEET 3 OF 3

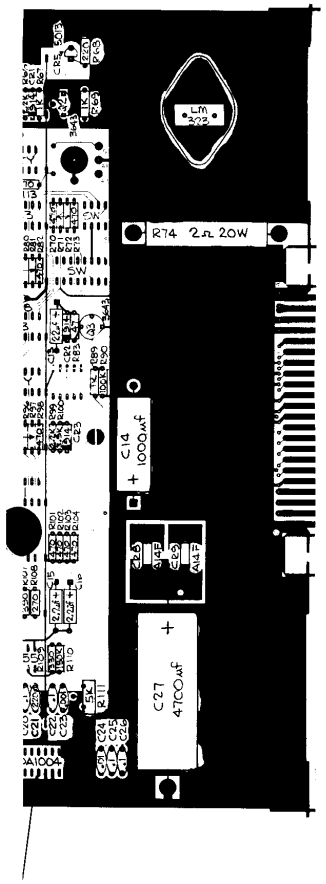
SCHEMATIC SIGNAL	FROM	TO	SIGNAL DESCRIPTION
128V	H8 (pin 11)	N8 (pin 1)	vertical timing signals place the window between horizontal scan lines 232 and 240. The horizontal timing signals place the window in the center of the TV monitor display and makes the width of the window equal to 128H.
64H	L3 (pin 11)	C6 (pin 5)	
128H	J3 (pin 14)	C6 (pin 4)	
256H	J3 (pin 13)	N8 (pin 12)	
$\overline{\text{V BLANK}}$	J7 (pin 11)	N8 (pin 6)	

ROADWAY SIGNALS

BD0	F3 (pins 2 & 4)	H6 (pin 4)	Data input to the vertical position read-only memory (VP RAMs H6, P6). In order to write vertical position data into the VP RAMs, $\overline{\text{POSV}}$ (H6, P6 pin 3) must be a low logic level. The address input is from the outputs of demodulator P5 (pins 4, 7, 9, and 12). During the V BLANK period, data is stored in these VP RAMs for the vertical position of all the roadway pylons.
BD1	E3 (pins 12 & 14)	H6 (pin 6)	
BD2	E3 (pins 2 & 4)	H6 (pin 10)	
BD3	F3 (pins 5 & 7)	H6 (pin 12)	
BD4	F3 (pins 12 & 14)	P6 (pin 4)	
BD5	E3 (pins 9 & 11)	P6 (pin 6)	
BD6	E3 (pins 5 & 7)	P6 (pin 10)	
BD7	F3 (pins 9 & 11)	P6 (pin 12)	
BD0	F3 (pins 2 & 4)	J6 (pin 4)	Data bus input to the horizontal position read-only memory (RAMs J6, L6). In order to write horizontal position data into the RAMs, $\overline{\text{POS H}}$ (J6, L6 pin 3) must be a low logic level. The address input is from the outputs of demodulator P5 (pins 4, 7, 9, and 12). During the V BLANK period, data is stored in these RAMs for the horizontal position of all of the roadway pylons.
BD1	E3 (pins 12 & 14)	J6 (pin 6)	
BD2	E3 (pins 2 & 4)	J6 (pin 10)	
BD3	F3 (pins 5 & 7)	J6 (pin 12)	
BD4	F3 (pins 12 & 14)	L6 (pin 4)	
BD5	E3 (pins 9 & 11)	L6 (pin 6)	
BD6	E3 (pins 5 & 7)	L6 (pin 10)	
BD7	F3 (pins 9 & 11)	L6 (pin 12)	
BD0	F3 (pins 2 & 4)	E6 (pin 4)	Data bus input to the character picture read-only memory (RAMs E6, M6). In order to write character picture data into the RAMs, CHAR must be a low logic level. The address input is from the outputs of demodulator P5 (pins 4, 7, 9, and 12.) During the V BLANK period, data is stored in these RAMs for the size and width (character picture) of the roadway pylons.
BD1	E3 (pins 12 & 14)	E6 (pin 6)	
BD2	E3 (pins 2 & 4)	E6 (pin 10)	
BD3	F3 (pins 5 & 7)	E6 (pin 12)	
BD4	F3 (pins 12 & 14)	M6 (pin 4)	
BD5	E3 (pins 9 & 11)	M6 (pin 6)	
BD6	E3 (pins 5 & 7)	M6 (pin 10)	
BD7	F3 (pins 9 & 11)	M6 (pin 12)	
BA4	C2 (pin 11)	K7 (pin 14)	Address signals BA4 and BA5 select the outputs of K7 as in the following table. If at any time HVC or BR/W is a low logic level, all of the outputs of K7 will be a low logic level.
BA5	C2 (pin 13)	K7 (pin 13)	
HVC	J2 (pin 3)	K8 (pin 9)	
BR/W	B4 (pin 13)	K8 (pin 10)	
$\overline{\text{COMP B}}$		L8 (pin 4)	Composite blanking signal. During the vertical blanking period and horizontal blanking period, this is a low logic level. During the horizontal scan period, this is a high logic level. Refer to Insert 8-1.

BA5	BA4	Decoder K7 output
L	L	POS H
L	H	POS V
H	L	CHAR
H	H	WATCH-DOG


132 TYP
18 PLACES
A006321
NIGHT DRIVER
ATARI © 76



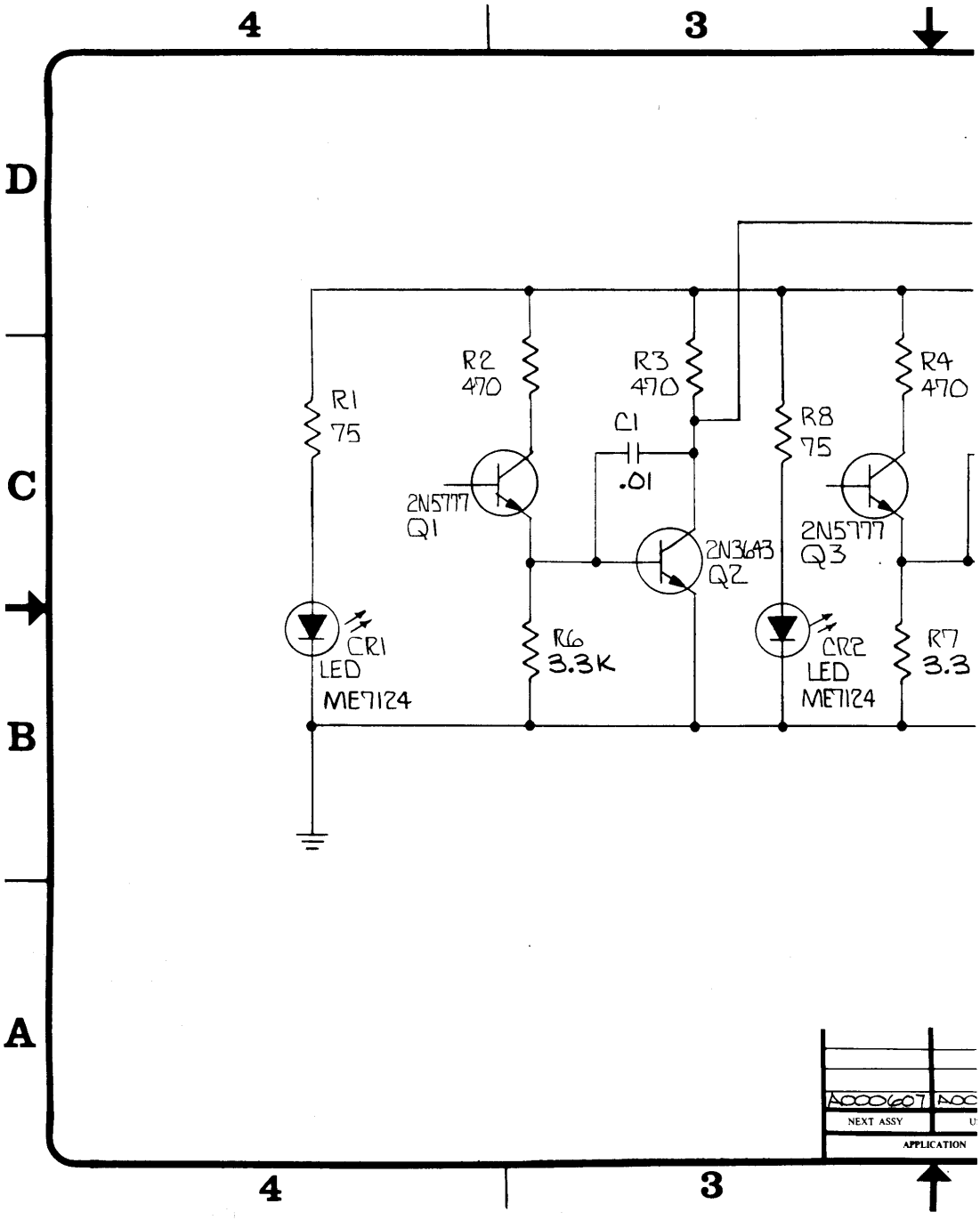
(128) HEATSINK
(129) ADHESIVE

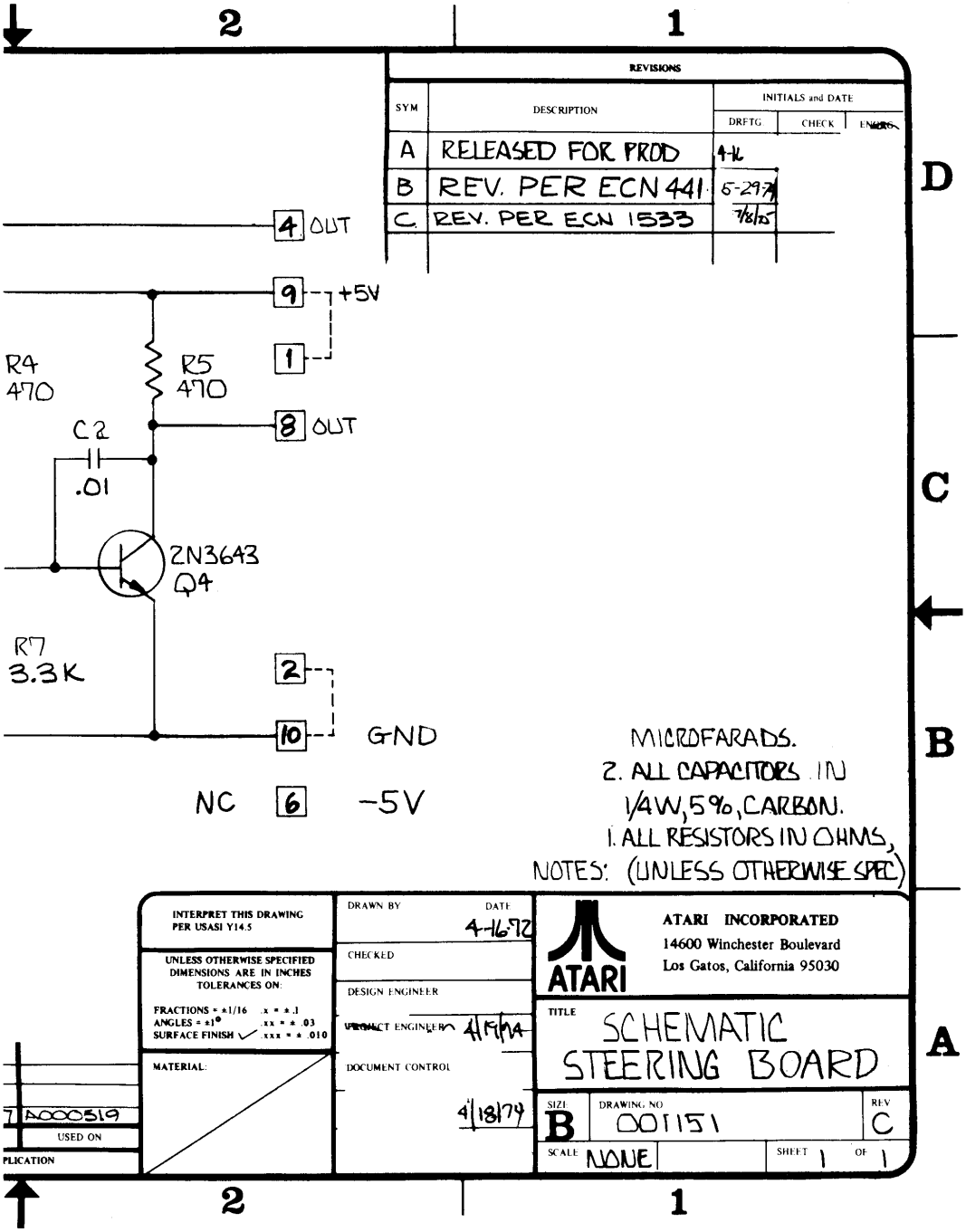
NOTES
1. USE THIS ASSEMBLY WITH 006322-01 REVISION "A" P.C. BOARDS.

MODIFICATIONS:
1. CUT AND LIFT PIN 3 OF J5 (7430).
2. JUMPER PIN 11 OF F8(9316) TO PIN 1 OF L8(7404).
3. JUMPER PIN 2 OF L8 TO PIN 3 OF J5.

OUTSTANDING ECNs	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: ANGLES = ±1° SURFACE FINISH ✓ .X = ±.1 .XX = ±.03 .XXX = ±.010	DO NOT SCALE DRAWING	ATARI INCORPORATED 14600 Winchester Boulevard Los Gatos, California 95030
MATERIAL: SEE P/L A006321-01	DRAWN BY DATE / CHECKED / ENGINEER	TITLE ASSEMBLY, NIGHT DRIVER P.C. BD
FINISH:	PROJECT ENGINEER / MFG ENGINEER	SIZE D · DRAWING NO. A006321-01 · REV A · SCALE 1:1 · SHEET 1 OF 1


4
3
D
C
B
A
R1
75
R2
470
R3
470
R4
470
C1
.01
R8
75
2N5777
Q1
2N3643
Q2
2N5777
Q3
CR1
LED
ME7124
R6
3.3K
CR2
LED
ME7124
R7
3.3
NEXT ASSY
APPLICATION


2
1
REVISIONS
SYM
DESCRIPTION
INITIALS and DATE
DRFTG
CHECK
A
RELEASED FOR PROD
4-16
B
REV. PER ECN 441
5-29-74
C
REV. PER ECN 1533
7/8/75
D
4 OUT
9 +5V
1
R4
470
R5
470
8 OUT
C2
.01
2N3643
Q4
R7
3.3K
2
10 GND
NC 6 -5V
C
B
MICROFARADS.
2. ALL CAPACITORS IN
1/4W, 5%, CARBON.
1. ALL RESISTORS IN OHMS,
NOTES: (UNLESS OTHERWISE SPEC)
INTERPRET THIS DRAWING PER USASI Y14.5
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON:
FRACTIONS = ±1/16 .x = ±.1
ANGLES = ±1° .xx = ±.03
SURFACE FINISH .xxx = ±.010
MATERIAL:
DRAWN BY
DATE
4-16-72
CHECKED
DESIGN ENGINEER
PRODUCT ENGINEER
4/15/74
DOCUMENT CONTROL
4/18/74
ATARI
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030
TITLE
SCHEMATIC
STEERING BOARD
A
SIZE
B
DRAWING NO
001151
REV
C
SCALE NONE
SHEET 1 OF 1
A000519
USED ON
PLICATION
2
1

ATARI

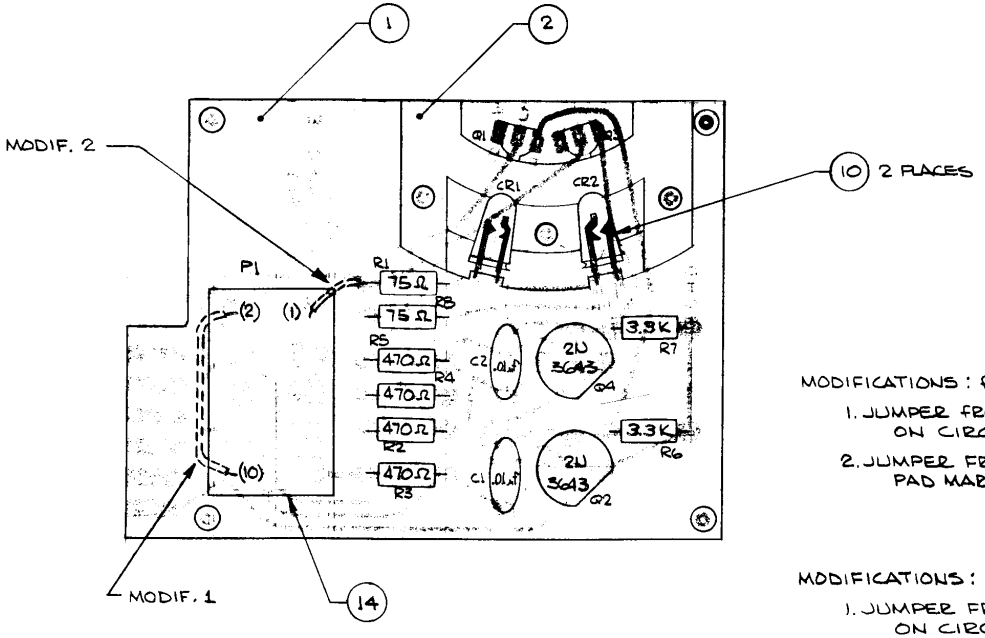
Job Title	Dwg.
RACETRAK STEERING PCB ASSY	P/L 000607

Parts List Specification **sheet 1 of** 1

Drawn		
Checked	Mech. Eng.	Rev.
Proj. Eng.	Elec. Eng.	
MF		M

Rev.	Description	Apprv.	Rev.	Description	Apprv.
H	Redesigned	5-6-74			
J	Rev per ECN 397	5/28/74			
K	Rev per ECN 457	6/3/74			
L	Rev per ECN 601	7/15/74			
M	Rev per ECN 1531				

Item	Part. No.	Qty.	Description
1	000614	1	Printed Circuit Board (E)
2	001092	1	Light Mount
3	001151	Ref	Schematic Diagram
4	11750/10-5750	2	Resistor, Comp., 75 ohm, ¼ watt, 5%
5	11471/10-5471	4	Resistor, Comp, 470 ohm, ¼ watt, 5%
6	11332/10-5332	2	Resistor, Comp, 3.3Kohm, ¼ watt, 5%
7	34104 /27-101103	2	Capacitor, Ceramic, .01uf
8	70006/38-2N5777	2	Transistor, 2N 5777 (Photo Darlington)
9	70000/34-2N3643	2	Transistor, 2N 3643
10	71008/38-ME7124	2	Light Emitting Diode, I.R. ME 7124
11			
12			
13			
14	80089 /79-58005	1	Connector, 10 pin, PC Mount, Amp #1-380991
15	72-1212S	1	Screw, Machine, Pan Head Phil, #2-56 x 3/4 Lg.
16	75-042	1	Washer, Split Lock #2
17	75-912S	1	Nut, Hex, #2-56
18	003749	1	Retainer, Led Light Mount



REFER TO SCHEMATIC 001151

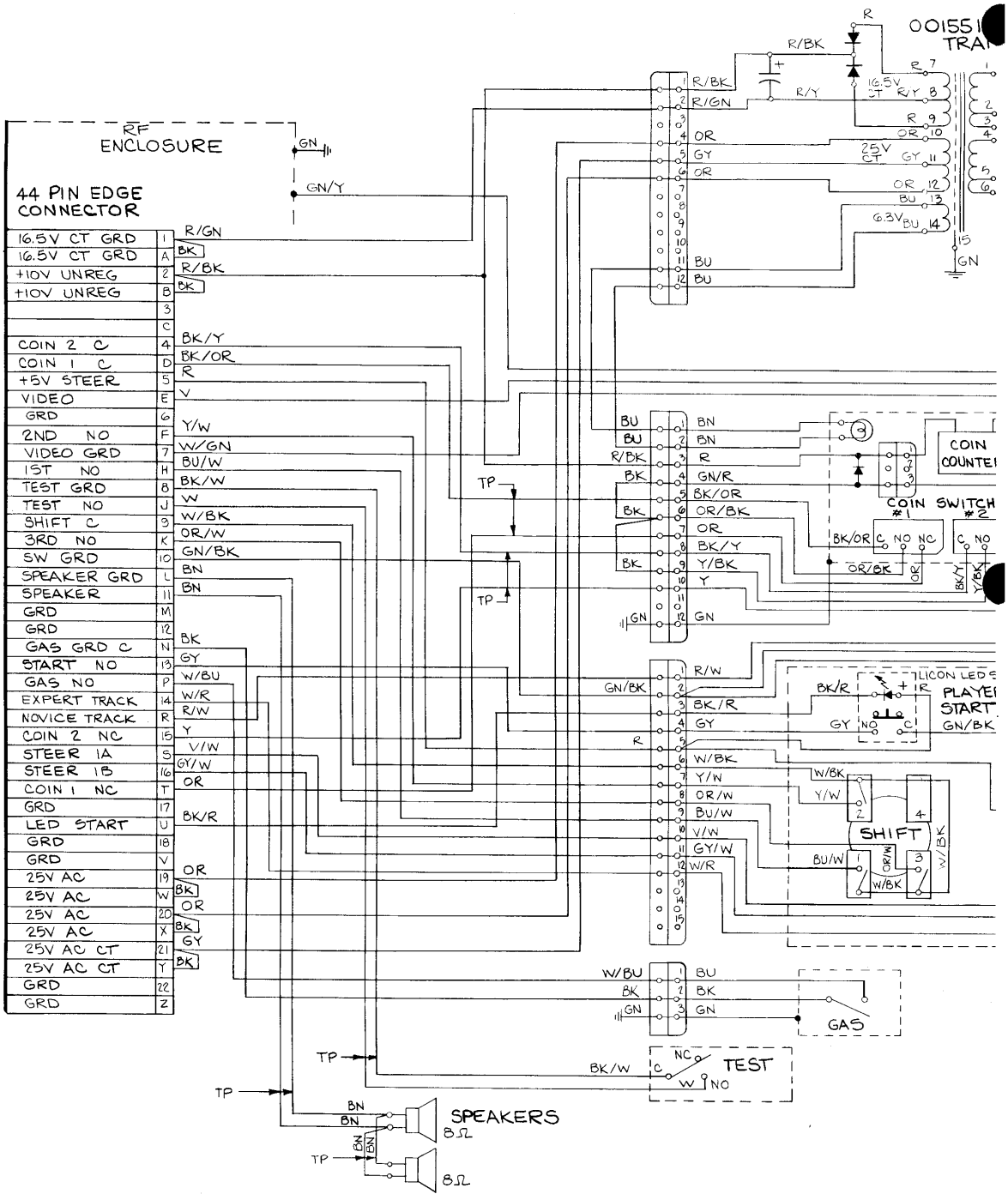
MODIFICATIONS: FOR 000614 REV J P.C. BOARDS

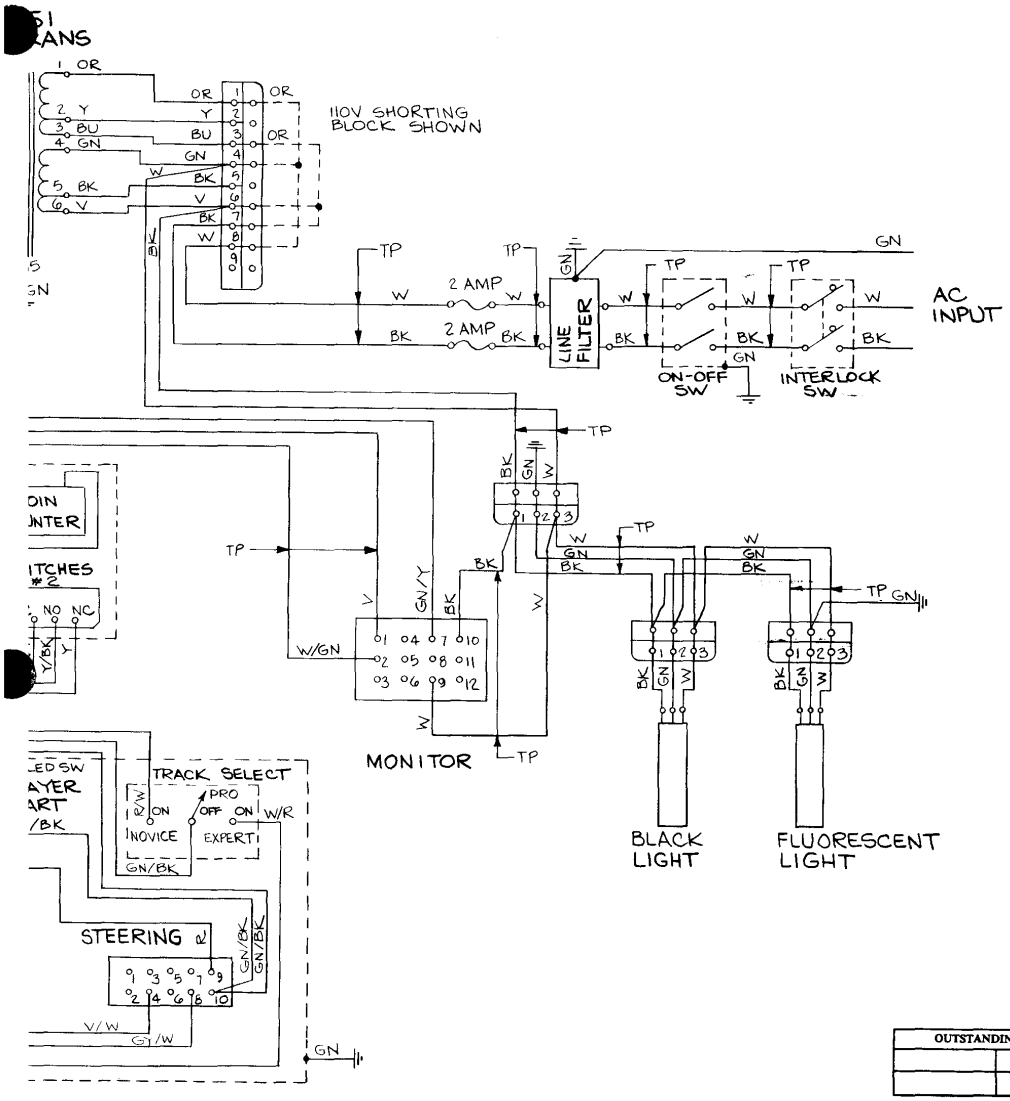
1. JUMPER FROM PIN 2 TO PIN 10 OF THE 10 PIN CONNECTOR, ON CIRCUIT SIDE OF BOARD.
2. JUMPER FROM PIN 1 OF THE 10 PIN CONNECTOR TO THE PAD MARKED +5V (END OF R1) ON CIRCUIT SIDE OF BOARD.

MODIFICATIONS: FOR 000614 REV K P.C. BOARDS.

1. JUMPER FROM PIN 2 TO PIN 10 OF THE 10 PIN CONNECTOR, ON CIRCUIT SIDE OF BOARD.

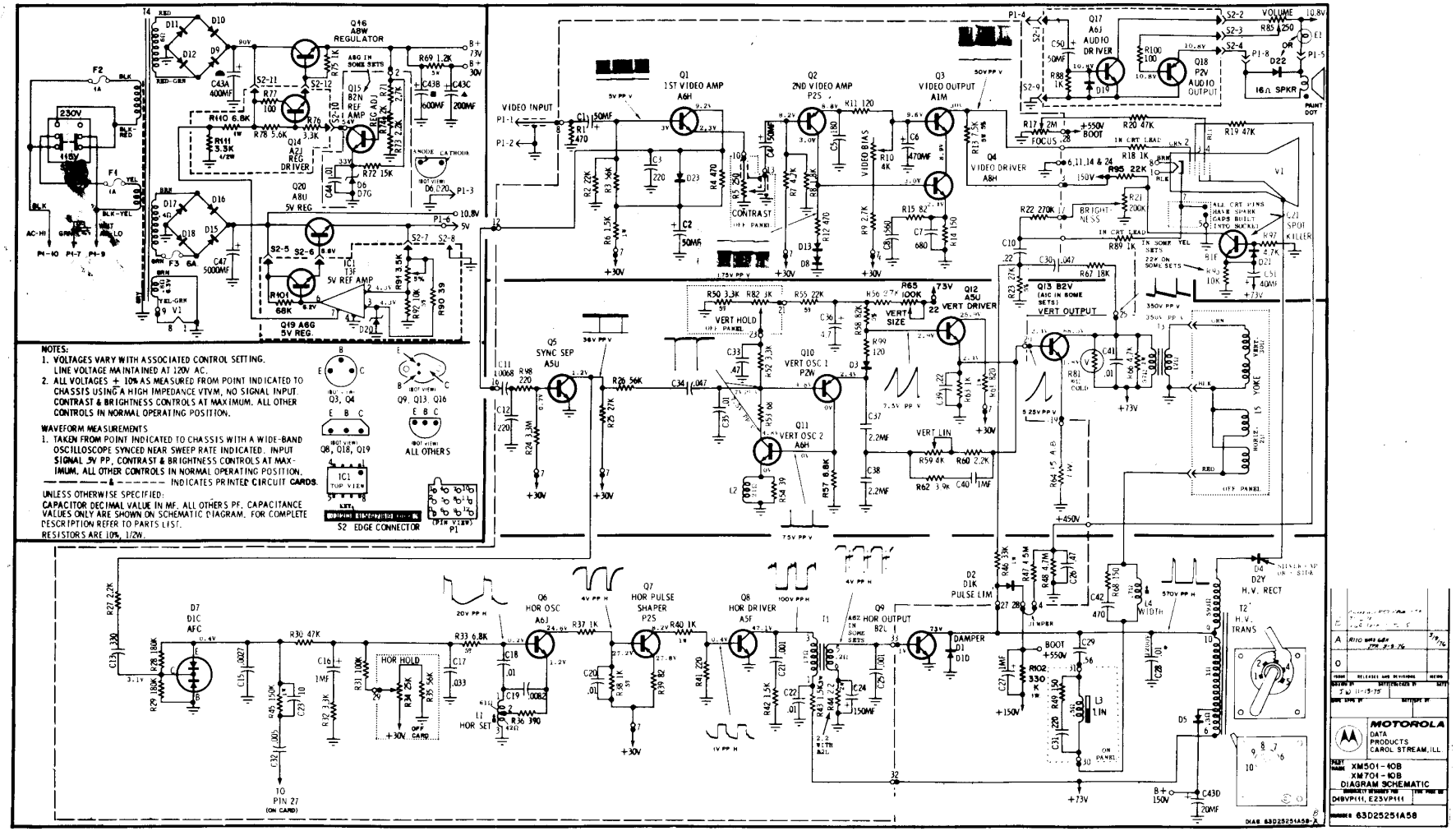
INTERPRET THIS DRAWING PER USASI Y14.5	DRAWN BY DATE	ATARI INCORPORATED 14600 Winchester Boulevard Los Gatos, California 95030
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: FRACTIONS = ±1/16 x = ± .1 ANGLES = ±1° xx = ± .03 SURFACE FINISH ✓ xxx = ± .010	CHECKED DESIGN ENGINEER PROJECT ENGINEER DOCUMENT CONTROL APPROVED	TITLE: ASSEMBLY STEERING BOARD
MATERIAL: SEE PL 000607		SIZE B · DRAWING NO A000607 · REV M SCALE 2:1 · SHEET 1 OF 1


RF ENCLOSURE
GN
GN/Y
44 PIN EDGE CONNECTOR
16.5V CT GRD 1
16.5V CT GRD A
+10V UNREG 2
+10V UNREG B
3
C
COIN 2 C 4
COIN 1 C D
+5V STEER 5
VIDEO E
GRD 6
2ND NO F
VIDEO GRD 7
1ST NO H
TEST GRD 8
TEST NO J
SHIFT C 9
3RD NO K
SW GRD 10
SPEAKER GRD L
SPEAKER 11
GRD M
GRD 12
GAS GRD C N
START NO 13
GAS NO P
EXPERT TRACK 14
NOVICE TRACK R
COIN 2 NC 15
STEER 1A S
STEER 1B 16
COIN 1 NC T
GRD 17
LED START U
GRD 18
GRD V
25V AC 19
25V AC W
25V AC 20
25V AC X
25V AC CT 21
25V AC CT Y
GRD 22
GRD Z
R/GN
BK
R/BK
BK
BK/Y
BK/OR
R
V
Y/W
W/GN
BU/W
BK/W
W
W/BK
OR/W
GN/BK
BN
BN
BK
GY
W/BU
W/R
R/W
Y
V/W
GY/W
OR
BK/R
OR
BK
OR
BK
GY
BK
R/BK
R/GN
OR
GY
OR
BU
BU
R/BK
R/Y
16.5V CT
25V CT
6.3V
GN
TP
TP
TP
TP
BU
BU
R/BK
BK
BK
BK
BK
GN
BN
BN
R
GN/R
BK/OR
OR/BK
OR
BK/Y
Y/BK
Y
GN
COIN COUNTE
COIN SWITCH #1 #2
BK/OR
OR/BK
BK/Y
Y/BK
R/W
GN/BK
BK/R
GY
R
W/BK
Y/W
OR/W
BU/W
V/W
GY/W
W/R
LICON LED
PLAYE START
GN/BK
SHIFT
W/BK
Y/W
BU/W
OR/W
W/BK
W/BU
BK
GN
BU
BK
GN
GAS
BK/W
TEST
NC
C
W
NO
SPEAKERS
8Ω
8Ω
BN
BN
BN
BN



OUTSTANDING ECNs	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: .x = ±.1, .xx = ±.03, .xxx = ±.010, ANGLES = ±1°, SURFACE FINISH	DO NOT SCALE DRAWING	ATARI INCORPORATED 14600 Winchester Boulevard Los Gatos, California 95030
	DRAWN BY / DATE	
MATERIAL:	CHECKED	TITLE: NIGHT DRIVER HARNESS SCHEMATIC
	ENGINEER	
FINISH:	PROJECT ENGINEER	SIZE D / DRAWING NO. 006543-01 / REV A
	MFG. ENGINEER	SCALE / SHEET / OF


NOTES:
1. VOLTAGES VARY WITH ASSOCIATED CONTROL SETTING. LINE VOLTAGE MAINTAINED AT 120V AC.
2. ALL VOLTAGES ± 10% AS MEASURED FROM POINT INDICATED TO CHASSIS USING A HIGH IMPEDANCE VTVM, NO SIGNAL INPUT. CONTRAST & BRIGHTNESS CONTROLS AT MAXIMUM. ALL OTHER CONTROLS IN NORMAL OPERATING POSITION.
WAVEFORM MEASUREMENTS
1. TAKEN FROM POINT INDICATED TO CHASSIS WITH A WIDE-BAND OSCILLOSCOPE SYNCED NEAR SWEEP RATE INDICATED. INPUT SIGNAL .5V PP, CONTRAST & BRIGHTNESS CONTROLS AT MAXIMUM. ALL OTHER CONTROLS IN NORMAL OPERATING POSITION.
INDICATES PRINTED CIRCUIT CARDS.
UNLESS OTHERWISE SPECIFIED:
CAPACITOR DECIMAL VALUE IN MF. ALL OTHERS PF. CAPACITANCE VALUES ONLY ARE SHOWN ON SCHEMATIC DIAGRAM. FOR COMPLETE DESCRIPTION REFER TO PARTS LIST.
RESISTORS ARE 10%, 1/2W.
Q3, Q4
Q9, Q13, Q16
Q8, Q18, Q19
ALL OTHERS
S2 EDGE CONNECTOR
P1
VIDEO INPUT
Q1 1ST VIDEO AMP A6H
Q2 2ND VIDEO AMP P2S
Q3 VIDEO OUTPUT A1M
Q4 VIDEO DRIVER A8H
Q17 A6J AUDIO DRIVER
Q18 P2V AUDIO OUTPUT
VOLUME
16Ω SPKR
CONTRAST
BRIGHTNESS
SPOT KILLER
Q5 SYNC SEP A5U
Q10 VERT OSC 1 P2W
Q11 VERT OSC 2 A6H
Q12 A5U VERT DRIVER
Q13 B2V (A1C IN SOME SETS) VERT OUTPUT
VERT HOLD
VERT SIZE
VERT LIN
YOKE
Q19 A6G 5V REG.
Q20 A8U 5V REG
IC1 T3F 5V REF AMP
Q14 A2J REG DRIVER
Q15 B2N REF AMP
Q16 A8W REGULATOR
D7 D1C AFC
Q6 HOR OSC A6J
Q7 HOR PULSE SHAPER P2S
Q8 HOR DRIVER A5F
Q9 A6Z HOR OUTPUT B2L
D2 D1K PULSE LIM
D4 D2Y H.V. RECT
T2 H.V. TRANS
L4 WIDTH
L3 LIN
HOR HOLD
HOR SET
DAMPER
BOOST +550V
FOCUS
SCREEN
+73V
+30V
+450V
B+ 150V
B+ 73V
B+ 30V
230V
115V
AC-HI
AC-LO
F1 1A
F2 1A
F3 6A
T4
S2-1
S2-2
S2-3
S2-4
S2-5
S2-6
S2-7
S2-8
S2-9
S2-10
S2-11
S2-12
P1-1
P1-2
P1-3
P1-4
P1-5
P1-6
P1-7
P1-8
P1-9
P1-10
MOTOROLA
DATA PRODUCTS
CAROL STREAM, ILL.
XM501-10B
XM704-10B
DIAGRAM SCHEMATIC
D4BVP111, E23VP111
63D25251A58