

APB™ Schematic Package

Supplement to the Operators Manual

NOTE

This staple temporarily holds the schematic package together. Remove the staple before using these schematics.



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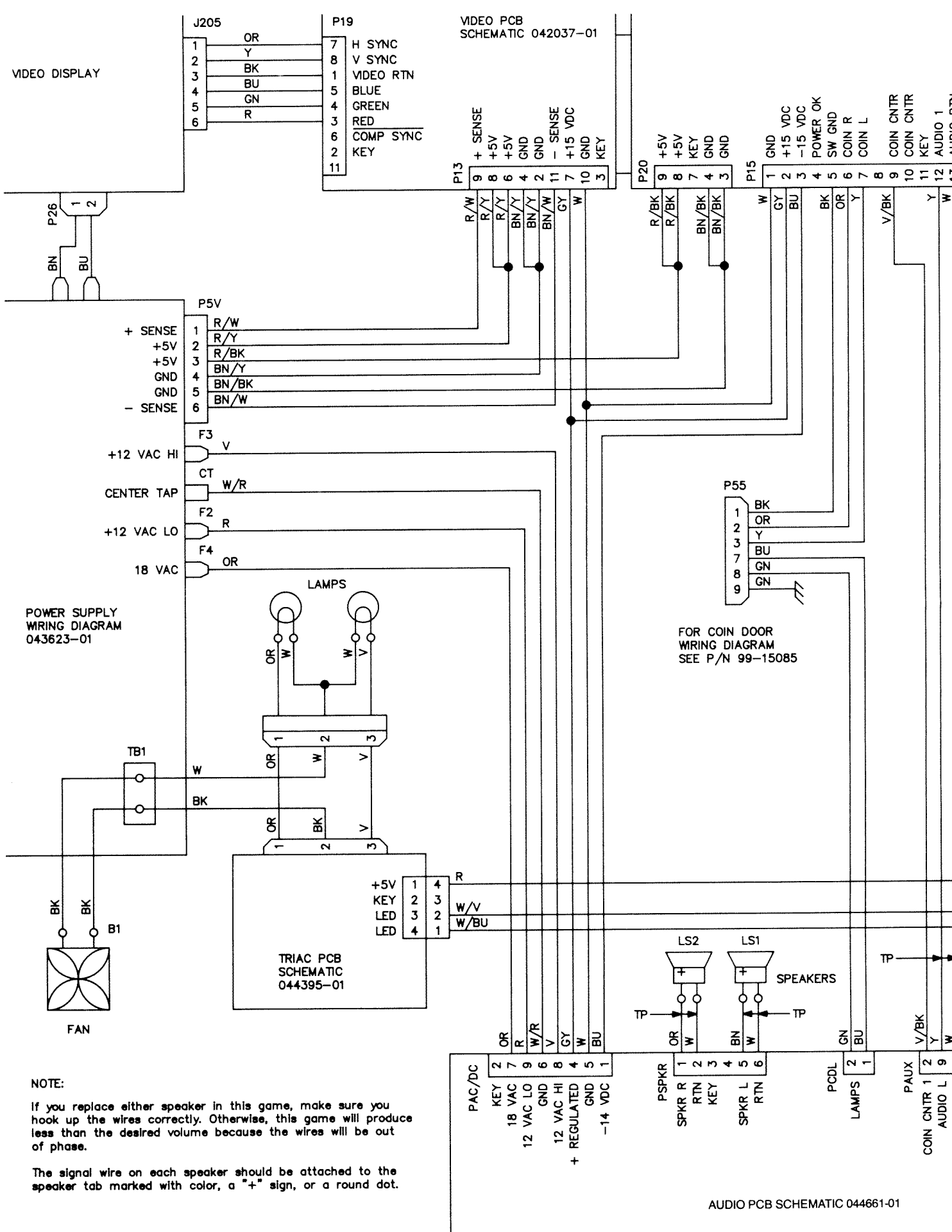
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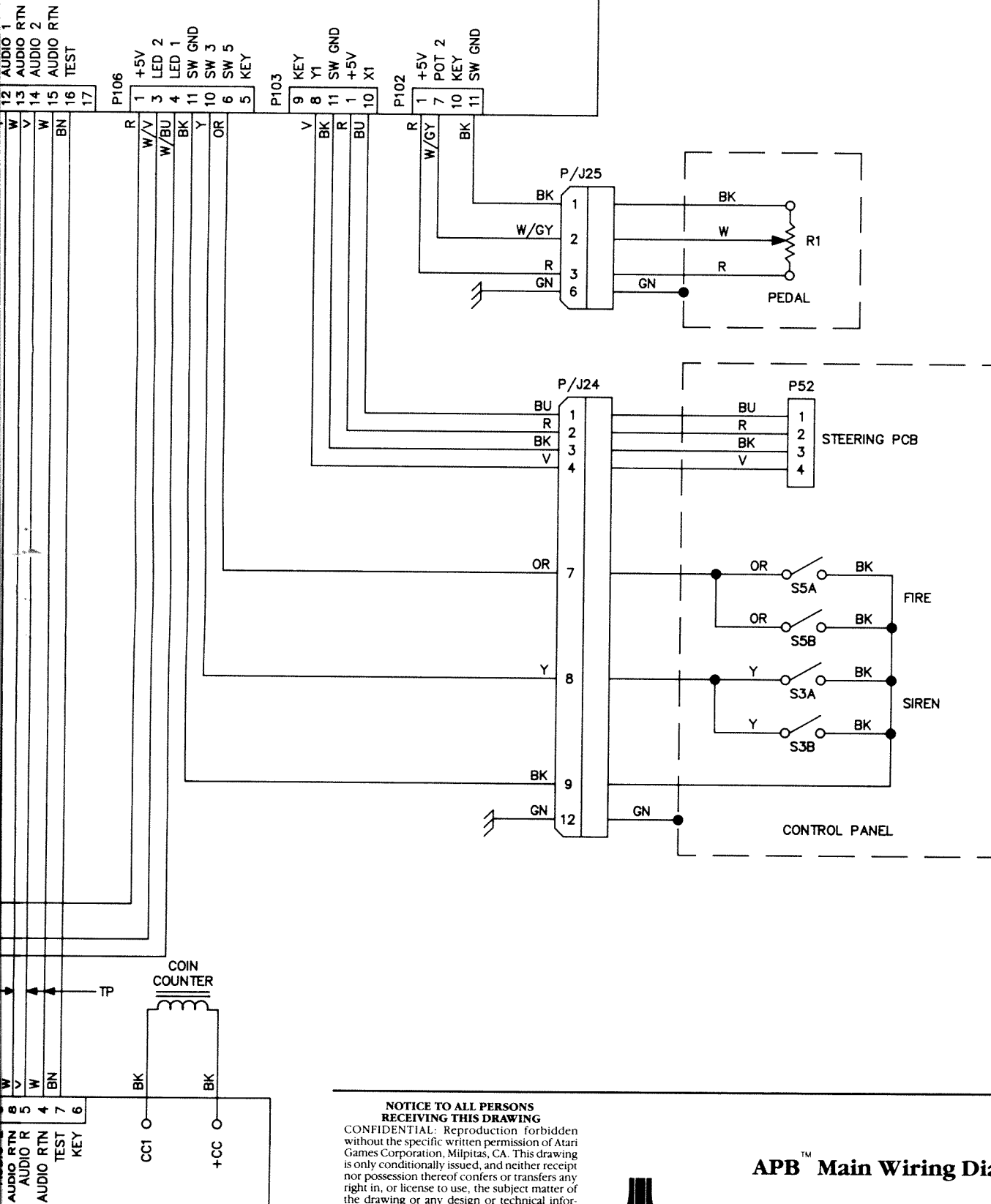
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NOTE:

If you replace either speaker in this game, make sure you hook up the wires correctly. Otherwise, this game will produce less than the desired volume because the wires will be out of phase.

The signal wire on each speaker should be attached to the speaker tab marked with color, a "+" sign, or a round dot.



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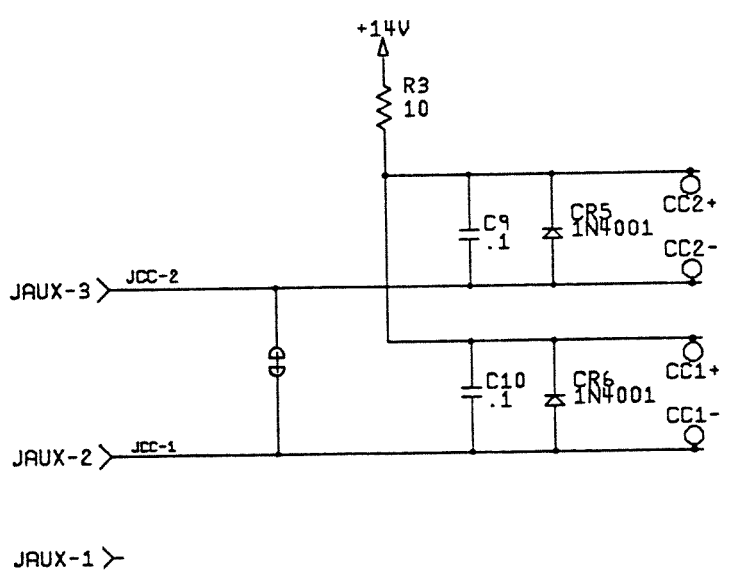
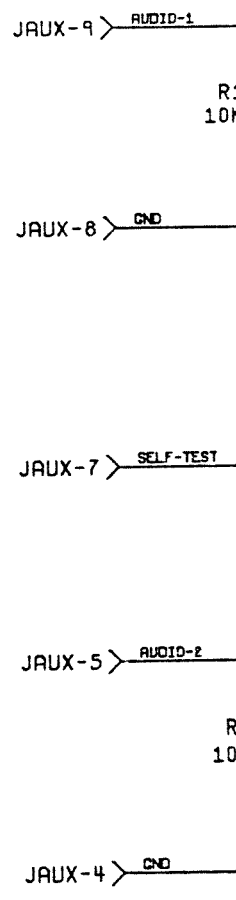
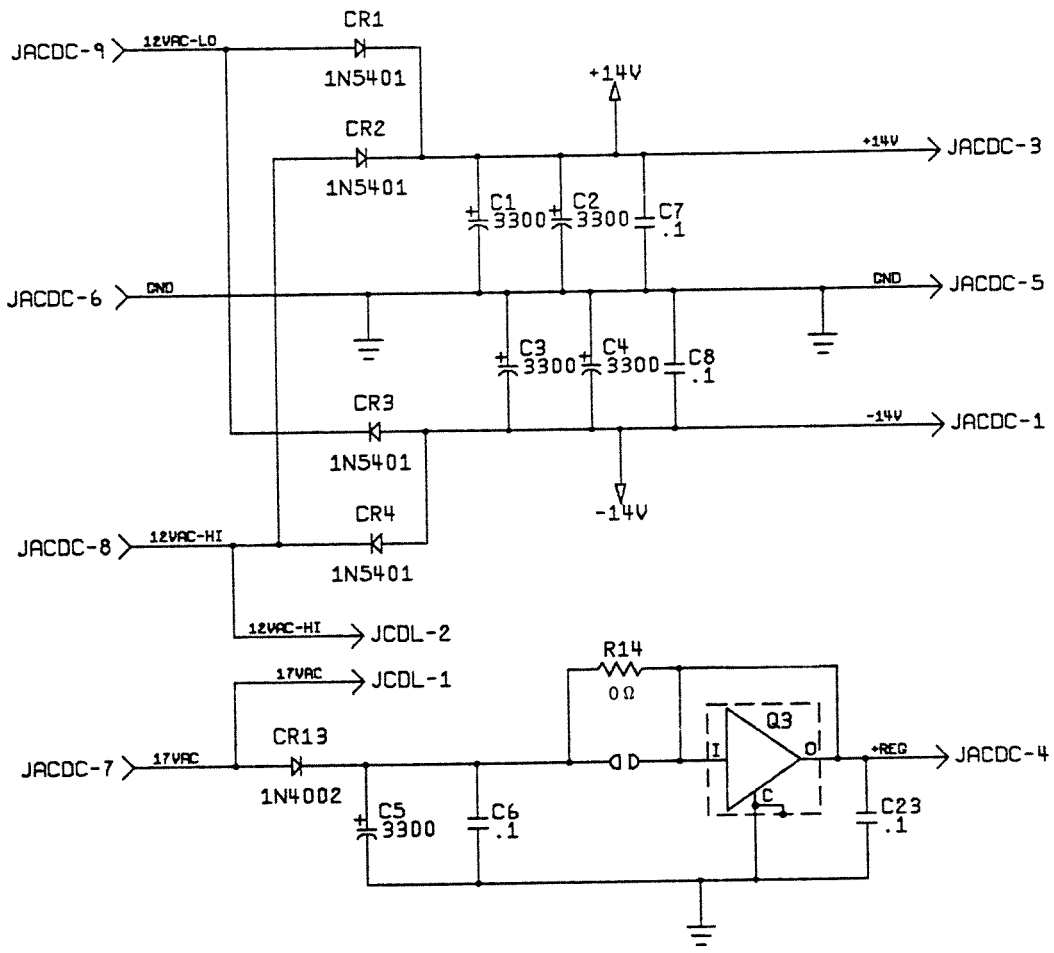
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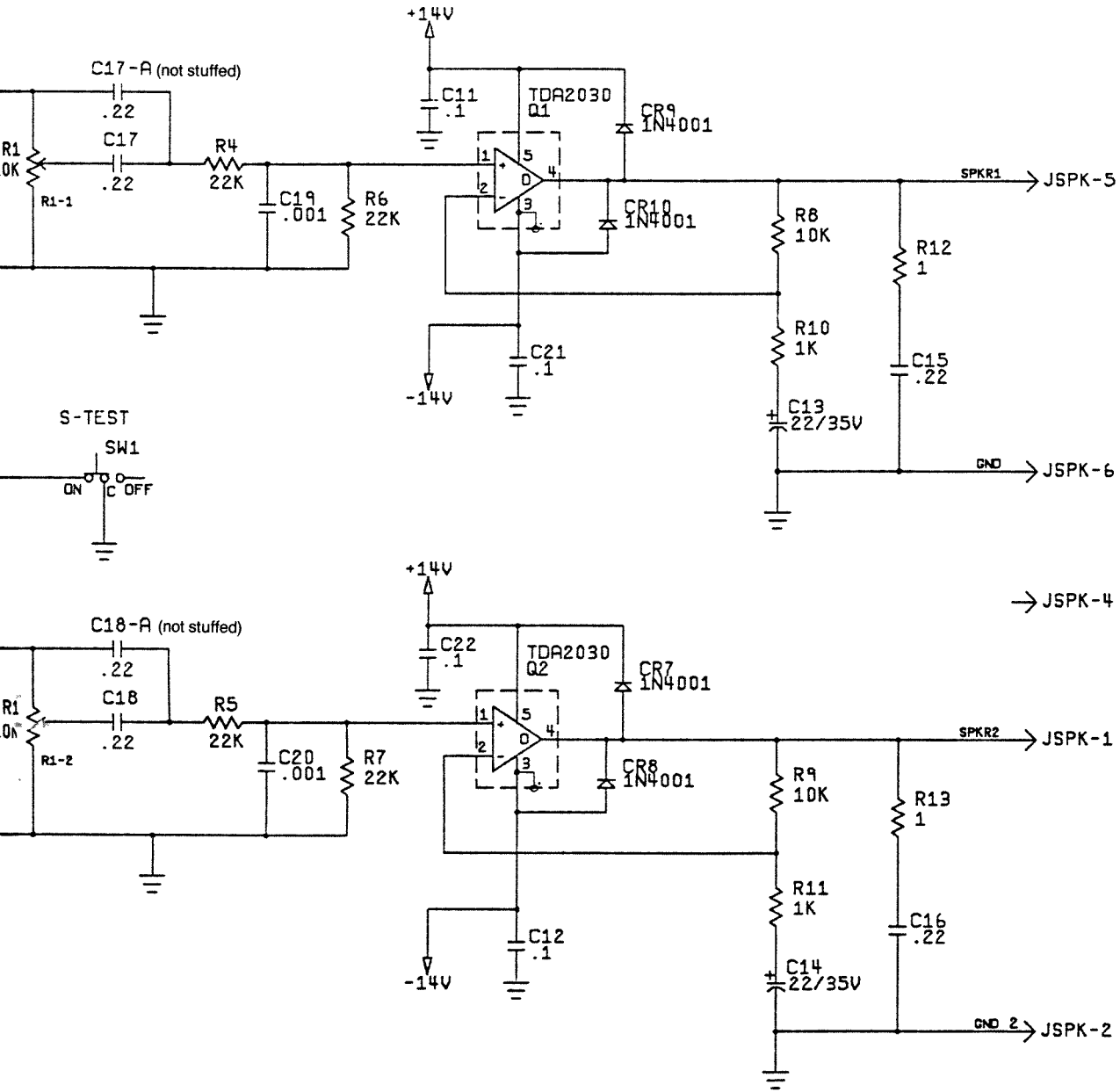
APB™ Main Wiring Diagram



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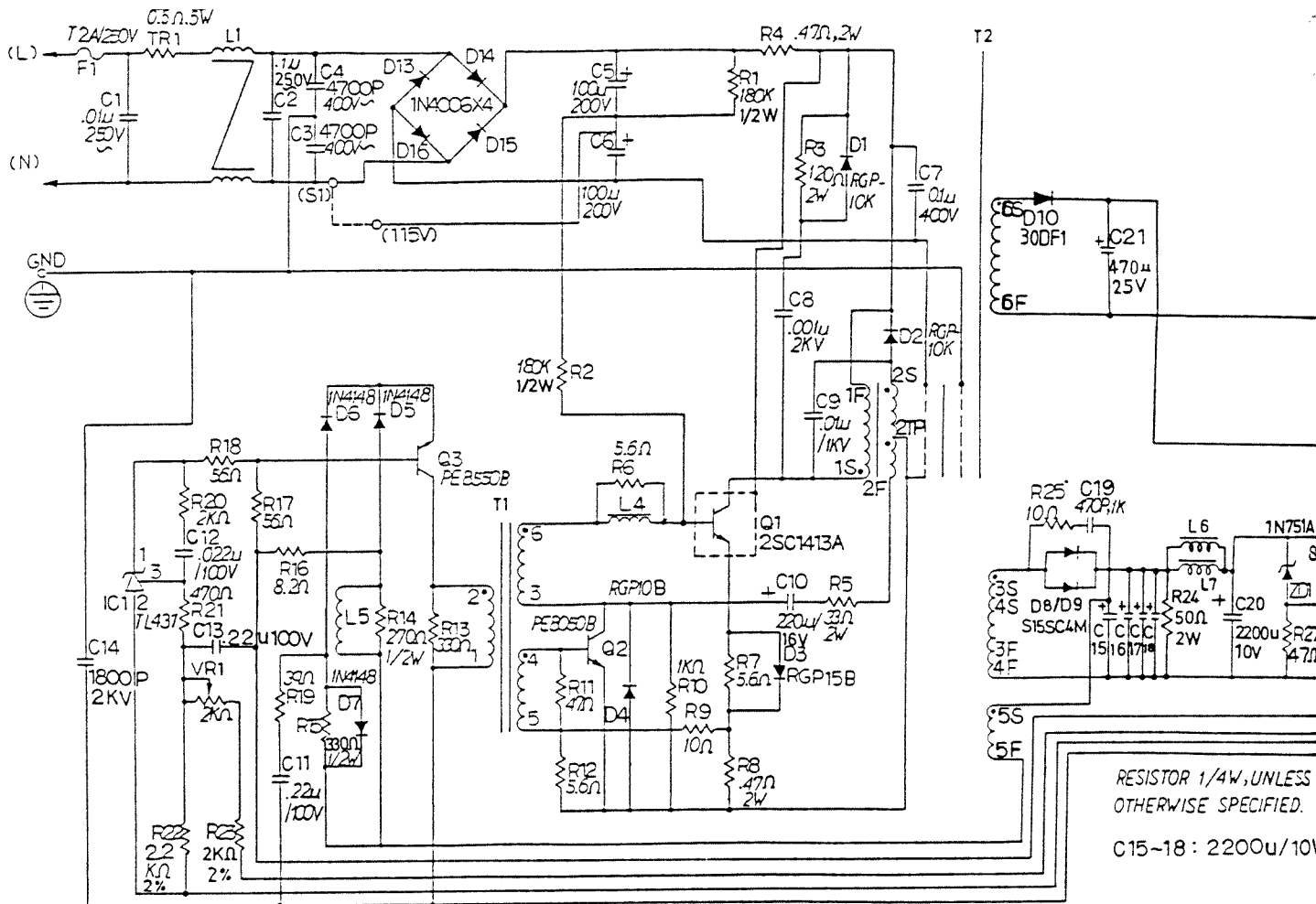
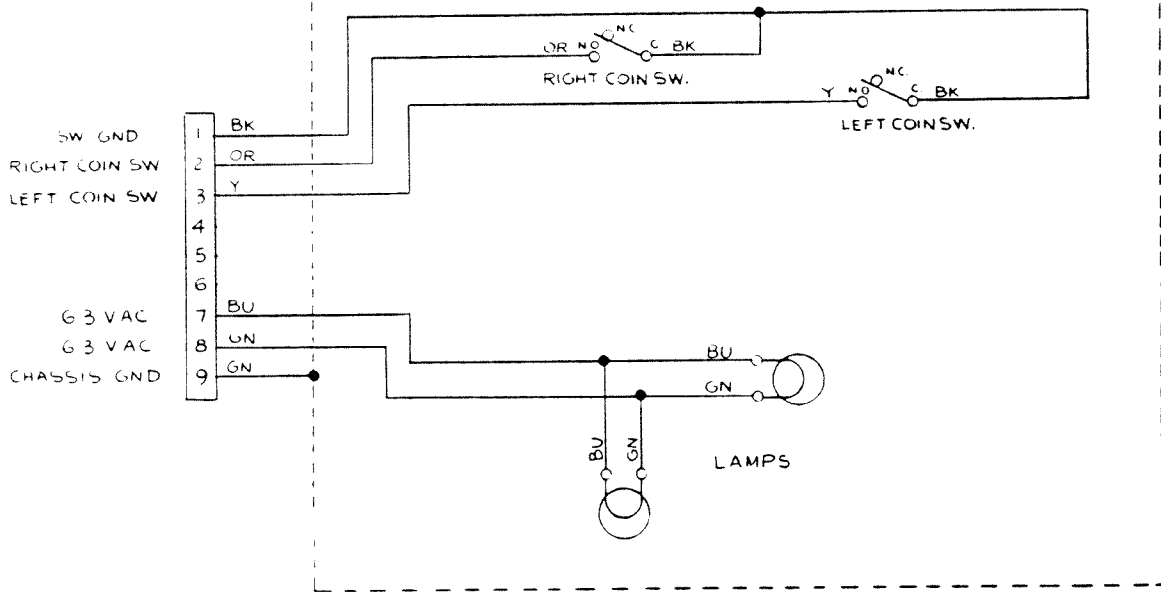


**APBTM Audio II
PCB Schematic Diagram**

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Coin Door Wiring Diagram



Hitron 5V, 13A Switching Power Supply

Main Microprocessor

Octal	Address Bus Signal Lines														R/W	Data					
	A	A	A	A	A	A	A	A	A	A	A	A	A	A		D	D	D			
	1	1	1	1	1	0	0	0	0	0	0	0	0	0		1	1	1			
	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0		5	4	3	2
000000-007777	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D
010000-010436	0	0	0	1	0	0	A	A	A	A	A	A	A	A	0		W	D	D	D	D
"	0	0	0	1	0	0	A	A	A	A	A	A	A	A	0		W				
"	0	0	0	1	0	0	A	A	A	A	A	A	A	A	0		W				
"	0	0	0	1	0	0	A	A	A	A	A	A	A	A	0		W				
010000-010176	0	0	0	1	0	0	0	0	A	A	A	A	A	A	0		W	D	D	D	D
010200-010276	0	0	0	1	0	0	0	1	A	A	A	A	A	A	0		W	D	D	D	D
010400-010776	0	0	0	1	0	0	1	0	0	0	A	A	A	A	0		W	D	D	D	D
012000	0	0	0	1	0	1	0	0	0	0					0		W	D	D	D	D
012002	0	0	0	1	0	1	0	0	0	0					1		W	D	D	D	D
012200	0	0	0	1	0	1	0	0	0	1							W				
012000-012002	0	0	0	1	0	1	0								A		R				
012400	0	0	0	1	0	1	0	1	0	1	0						W			D	D
012600	0	0	0	1	0	1	0	1	0	1	1	0	0				W				
012640	0	0	0	1	0	1	0	1	0	1	1	0	1				W				
012700	0	0	0	1	0	1	0	1	0	1	1	1	0				W				
012740	0	0	0	1	0	1	0	1	0	1	1	1	1				W				
013000	0	0	0	1	0	1	1	0	0								W				
013000	0	0	0	1	0	1	1	0	0								W				
013000	0	0	0	1	0	1	1	0	0								W				
013000	0	0	0	1	0	1	1	0	0								W				
013200	0	0	0	1	0	1	1	0	1								W				
013400	0	0	0	1	0	1	1	1	0								W	D	D	D	D
013600	0	0	0	1	0	1	1	1	1								W	D	D	D	D
014000	0	0	0	1	1	0	0	0	0								R				
014000	0	0	0	1	1	0	0	0	0								R				
014000	0	0	0	1	1	0	0	0	0								R				
014000	0	0	0	1	1	0	0	0	0								R				
014000	0	0	0	1	1	0	0	0	0								R				
014000	0	0	0	1	1	0	0	0	0								R				
014000	0	0	0	1	1	0	0	0	0								R				
014000	0	0	0	1	1	0	0	0	0								R	D			
016000	0	0	0	1	1	1	0	0	0								R				
020000-033776	0	0	1	A	A	A	A	A	A	A	A	A	A	A	A	0	R/W	D	D	D	D
"	0	0	1	A	A	A	A	A	A	A	A	A	A	A	A	0	R/W				
034000-037776	0	0	1	1	1	A	A	A	A	A	A	A	A	A	A	0	R/W	D	D	D	D
"	0	0	1	1	1	A	A	A	A	A	A	A	A	A	0	0	R/W	D	D	D	D
"	0	0	1	1	1	A	A	A	A	A	A	A	A	0	1	0	R/W	D	D	D	D
"	0	0	1	1	1	A	A	A	A	A	A	A	A	1	0	0	R/W	D	D	D	D
"	0	0	1	1	1	A	A	A	A	A	A	A	A	1	1	0	R/W	D	D	D	D
020000-037776	0	0	1	A	A	A	A	A	A	A	A	A	A	A	A	0	R/W	D	D	D	D
020000-037776	0	0	1	A	A	A	A	A	A	A	A	A	A	A	A	0	R/W	D	D	D	D
040000-057776	0	1	0	A	A	A	A	A	A	A	A	A	A	A	A	0	R	D	D	D	D
060000-077776	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	0	R	D	D	D	D
100000-177776	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	0	R	D	D	D	D

or (T-11) Memory Map

Data Bus Signal Lines	Function and Size
1 1 1 0 0 0 0 0 0 0 0 0 0 0	
2 1 0 9 8 7 6 5 4 3 2 1 0	
D D D D D D D D D D D D D D	Program RAM (4KB)
D D D D D D D D D D D D D D	Color RAM (144W)
D D D D	Z (Intensity)
D D D D	Blue
D D D D	Green
D	Red
D D D D D D D D D D D D D D	Motion Object Color RAM (64W)
D D D D D D D D D D D D D D	Alphanumeric Color RAM (16W)
D D D D D D D D D D D D D D	Playfield Color RAM (128W)
D D D	Program Page 0 Address
D D D	Program Page 1 Address
D D D D D D D D D D	A/D Converter Start Strobe
D	A/D Converter Output
D	Video Memory Page Select (VMMU)
D	IRQ0 Clear
D	6502 Reset
D	IRQ2 Clear
D	IRQ3 Clear
D	IRQ0 Enable 6502 RD (Active High)
D	IRQ1 Enable 6502 WT (Active High)
D	IRQ2 Enable 32V (Active High)
D	IRQ3 Enable VBLANK (Active High)
D D D D D D D D D D	Communications Port Write
D D D D D D D D D D	Horizontal Scroll & PF Bank 0
D D D D D D D D D D	Vertical Scroll & PF Bank 1
D	SW 6 (Active Low)
D	SW 5 (Active Low)
D	SW 4 (Active Low)
D	SW 3 (Active Low)
D	6502 Comm. Flag (Active High)
D	T-11 Comm. Flag (Active High)
D	SW 2 (Active Low)
D	SW 1 (Active Low)
D	Self-Test (Active Low)
D D D D D D D D D D	Communications Port Read
D D D D D D D D D D D D D D	Alphanumerics RAM (VMMU=0) (3KW)
D D D D D D D D D D D D D D	ANPIC
D D D D D D D D D D D D D D	Motion Object RAM (VMMU=0) (1KW)
D D D D D D D D D D D D D D	MOV
D D D D D D D D D D D D D D	MOPIC
D D D D D D D D D D D D D D	MOH
D D D D D D D D D D D D D D	MOLNK
D D D D D D D D D D D D D D	Playfield RAM Top (VMMU=2) (4KW)
D D D D D D D D D D D D D D	Playfield RAM Bottom (VMMU=3) (4KW)
D D D D D D D D D D D D D D	Paged Program (Page 0) (4KW)
D D D D D D D D D D D D D D	Paged Program (Page 1) (4KW)
D D D D D D D D D D D D D D	Program ROM (16KW)

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**APB™ Main
Microprocessor Memory Map**

Processor (6502) Memory Map

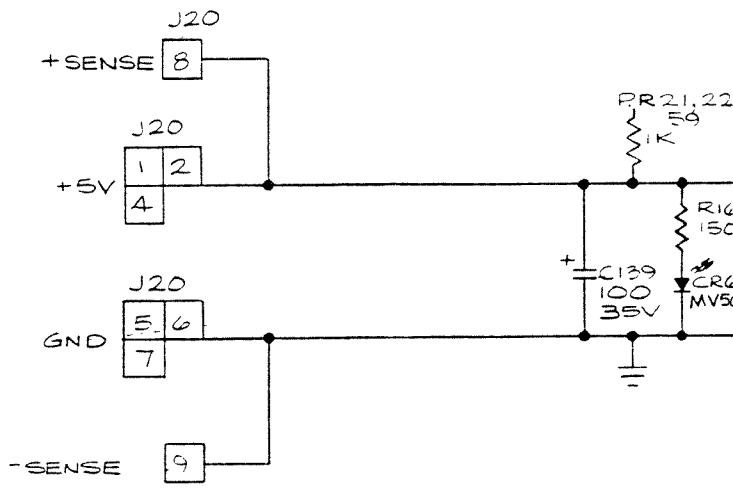
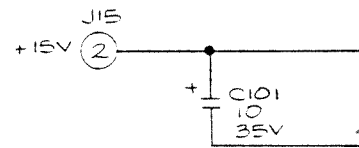
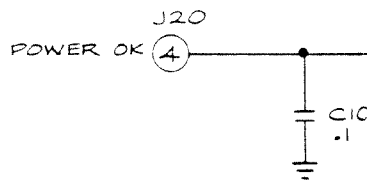
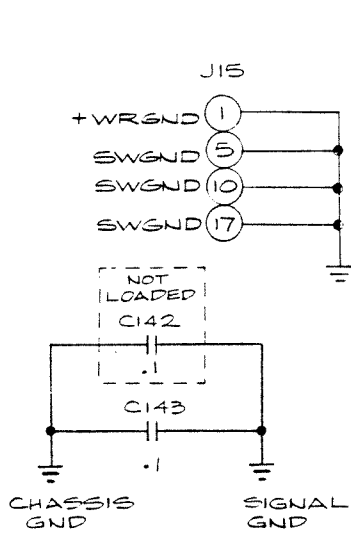
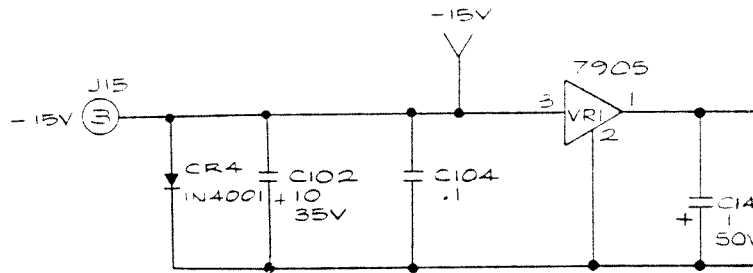
Address	Function and Size
DDDDDDDD	Program RAM (4KB)
00000000	EEROM (2KB)
76543210	POKEY 1 (16B)
	LETA
	POKEY 2 (16B)
	T-11 Talk (Active High)
	6502 Talk (Active High)
	TI READY (Active High)
	Self-Test Switch (Active Low)
	Auxiliary Coin Switch (Active Low)
	Left Coin Switch (Active Low)
	Right Coin Switch (Active Low)
	Yamaha Sound Chip
	Communications Port Read
	TI Data
	TI Write Enable
	Communications Port Write
	Right Coin Counter (Active High)
	Left Coin Counter (Active High)
	IRQ Clear
	Yamaha Mixer
	POKEY Mixer
	TI Sound Mixer
	LED 1
	LED 2
	LETA Resolution
	TI Frequency Select
	Sound Enable (Active High)
	Program ROM (16KB)
	Program ROM (32KB)

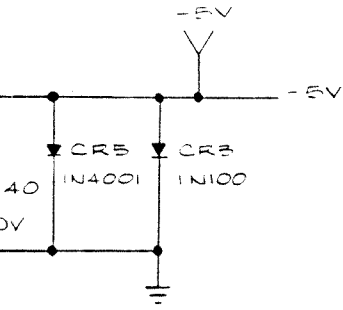
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**APB™ Sound
Microprocessor Memory Map**



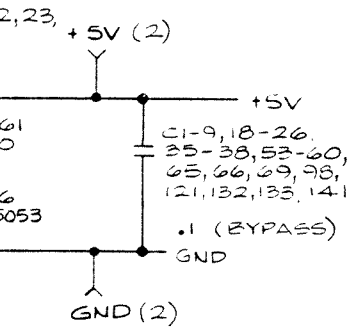
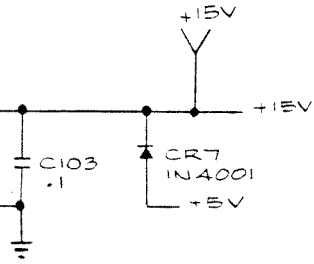


NOTES:

- CONNECTOR J20
- CONNECTOR P18
- CONNECTOR J15

POWER OK

05



Power Input

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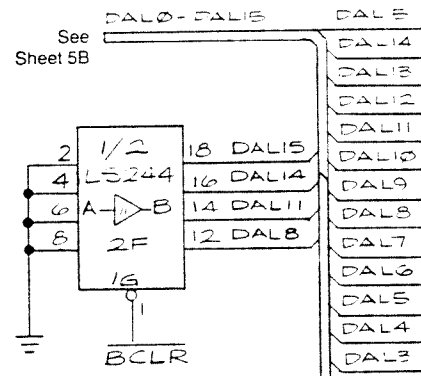
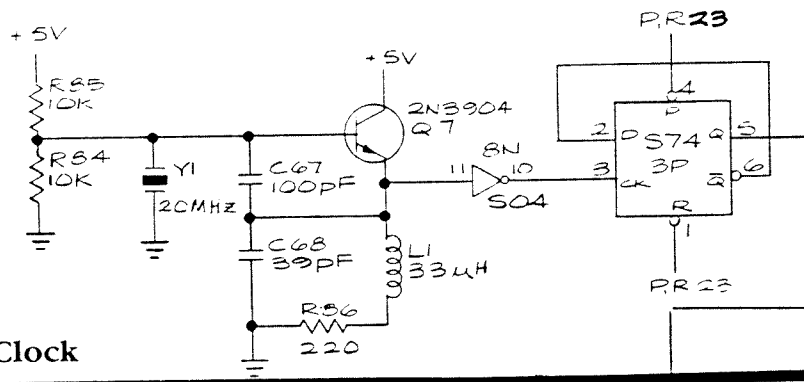


APB™ CPU PCB
Schematic Diagram

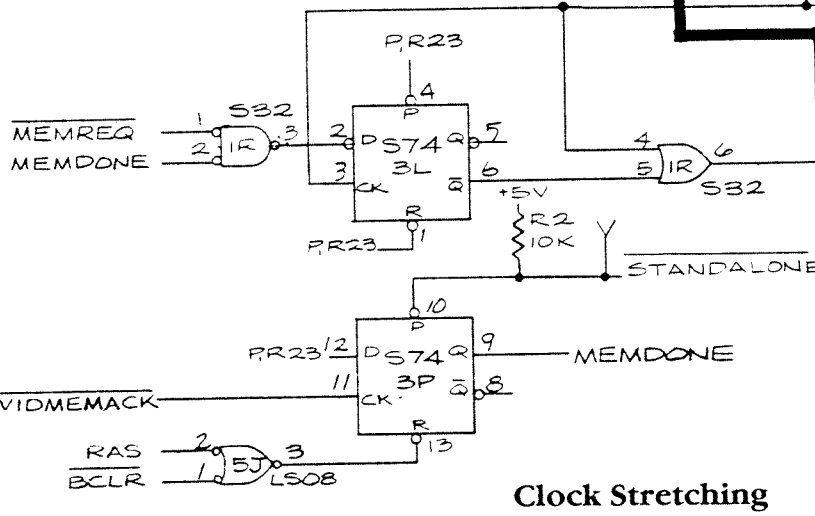
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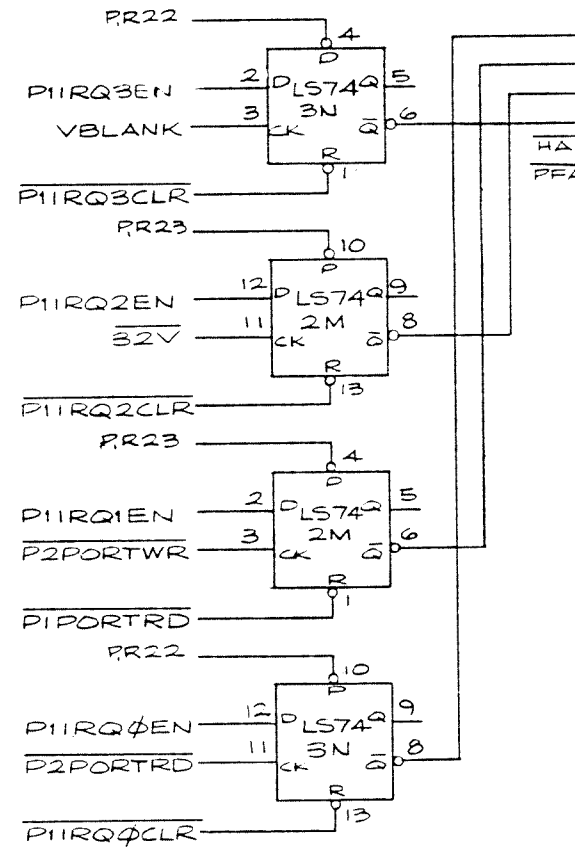
T-11 Clock



Mode Register

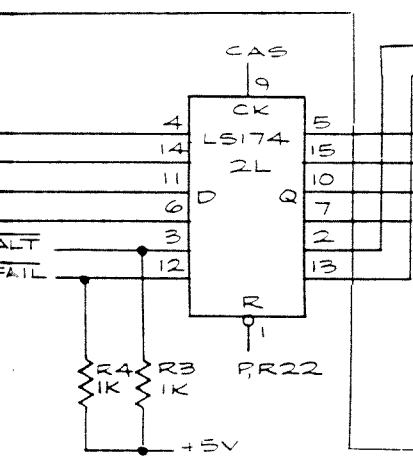


Clock Stretching

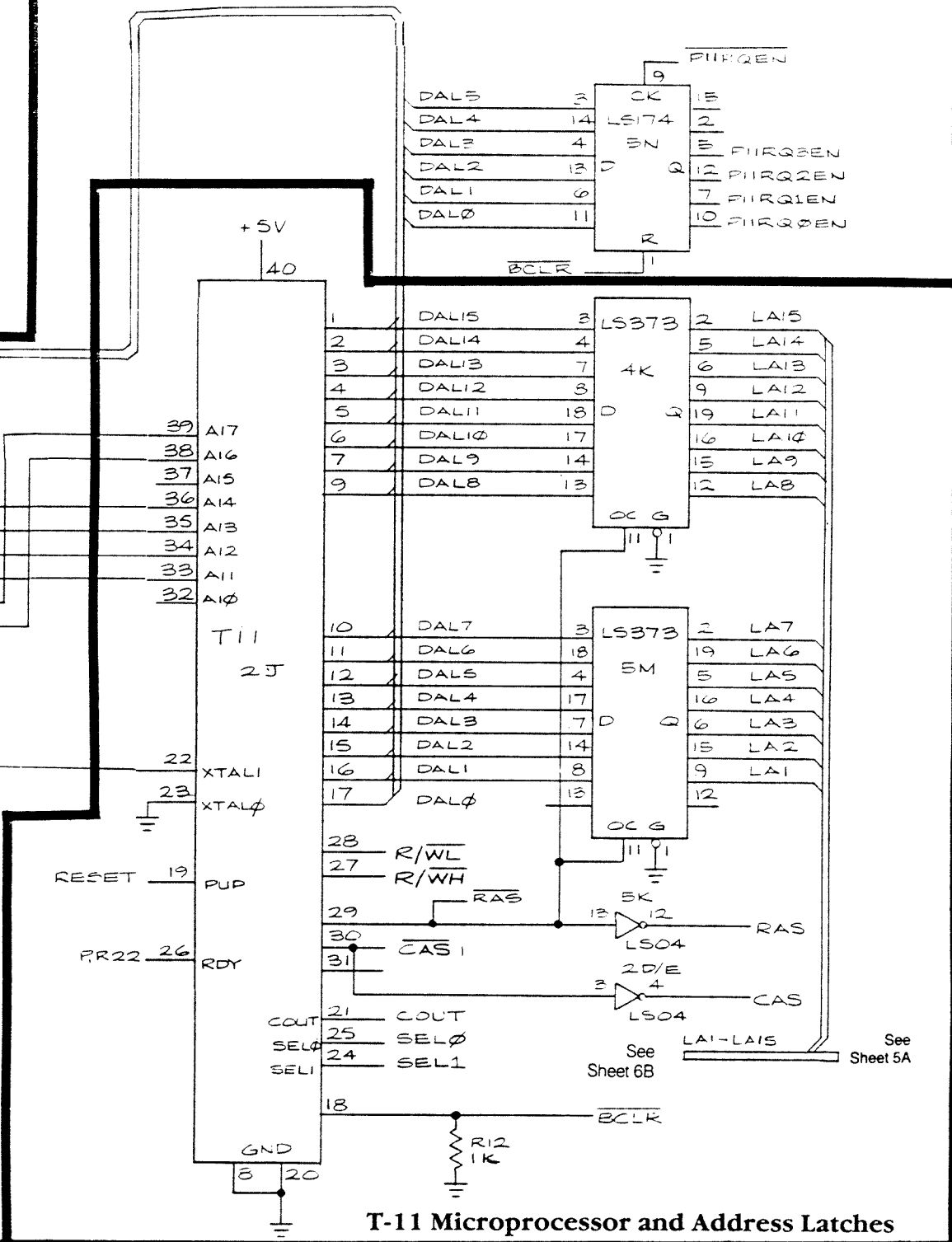


Extender Socket

1	EXTENDER	28	+5V
2	SOCKET	27	COUT
3	IF	26	RESET
4		25	HALT
5		24	FEATL
6		23	SEL1
7		22	SEL0
8		21	R/WL
9		20	R/WH
10		19	CAS
11		18	RAS
12		17	DAL0
13		16	DAL1
14		15	DAL2



Interrupt Logic



T-11 Microprocessor and Address Latches

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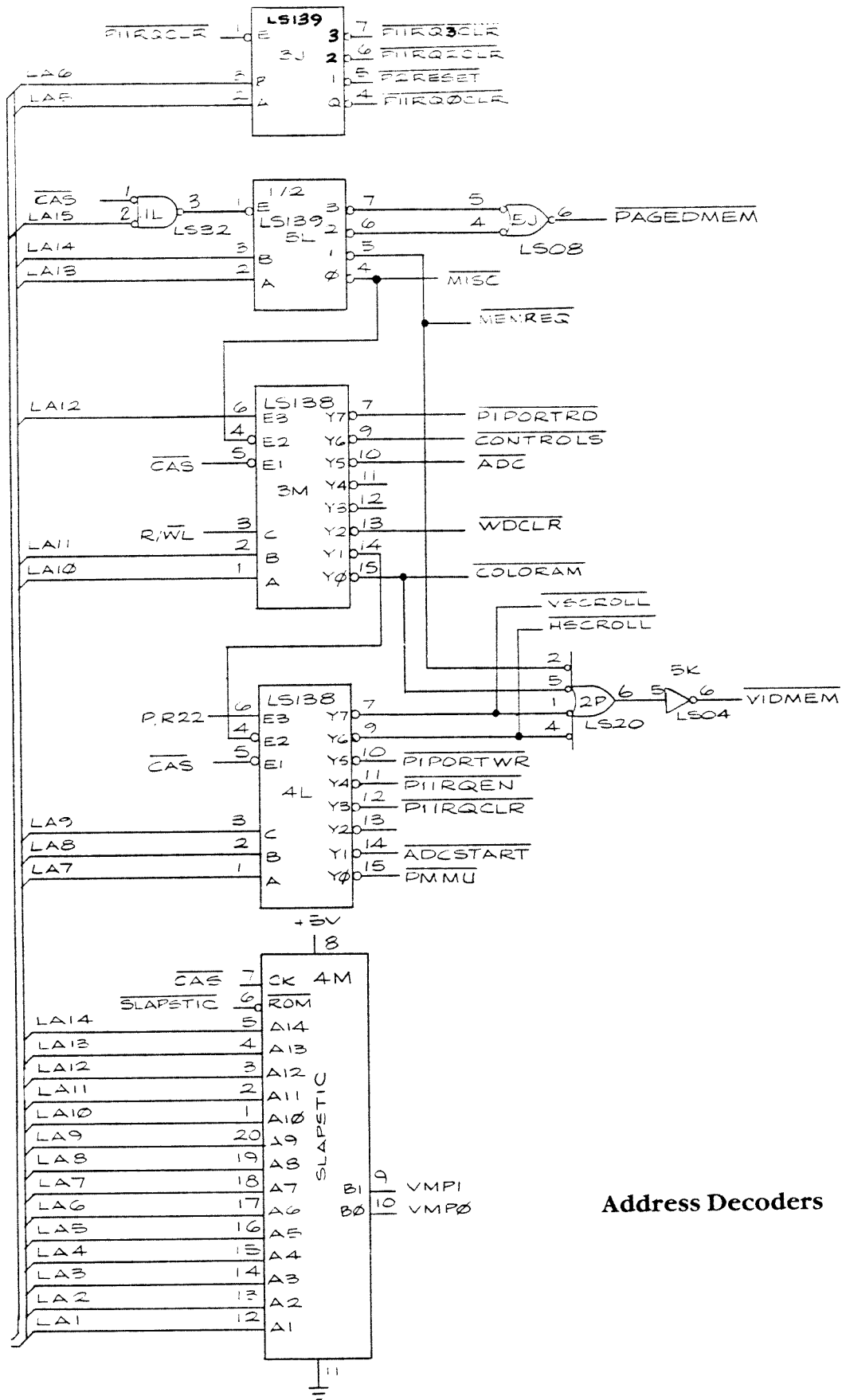
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APB™ CPU PCB Schematic Diagram

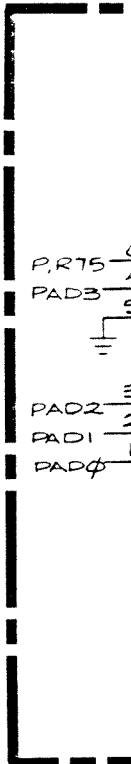
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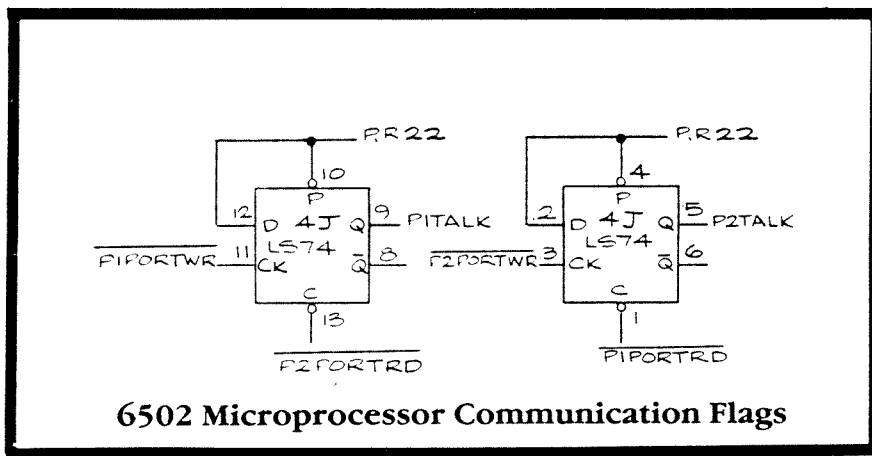
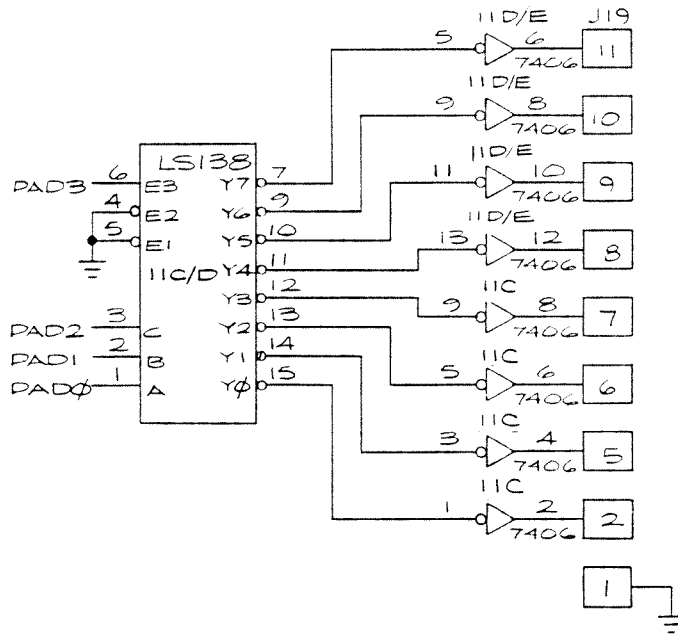
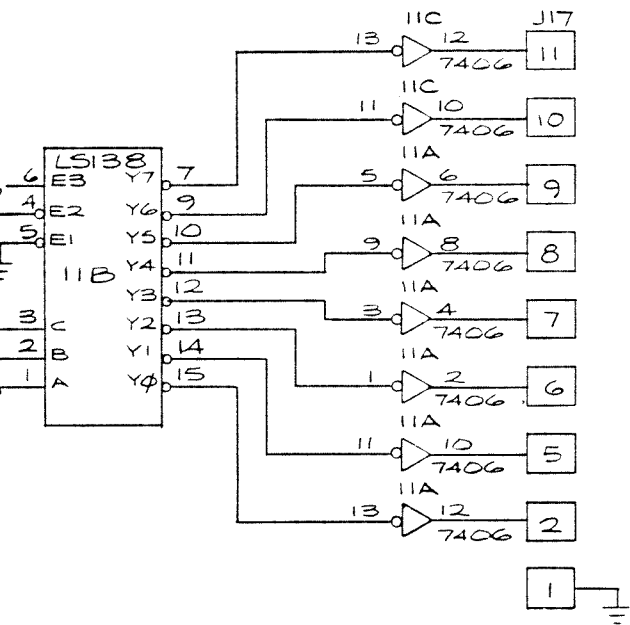


Address Decoders

See
Sheets
5B & 6A



Used in Development Only



6502 Microprocessor Communication Flags

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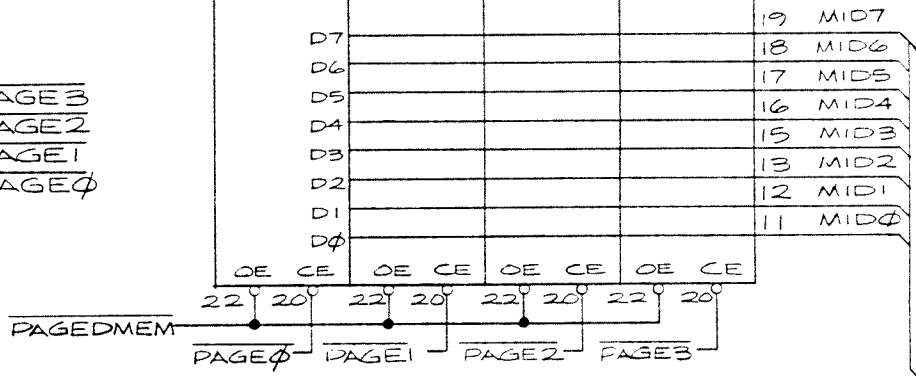
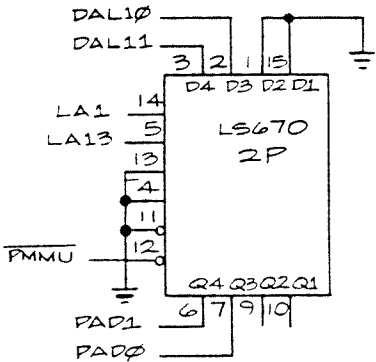
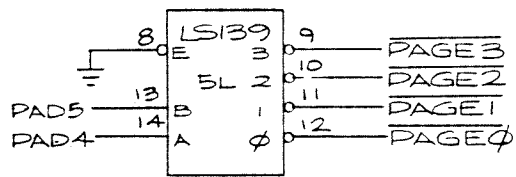
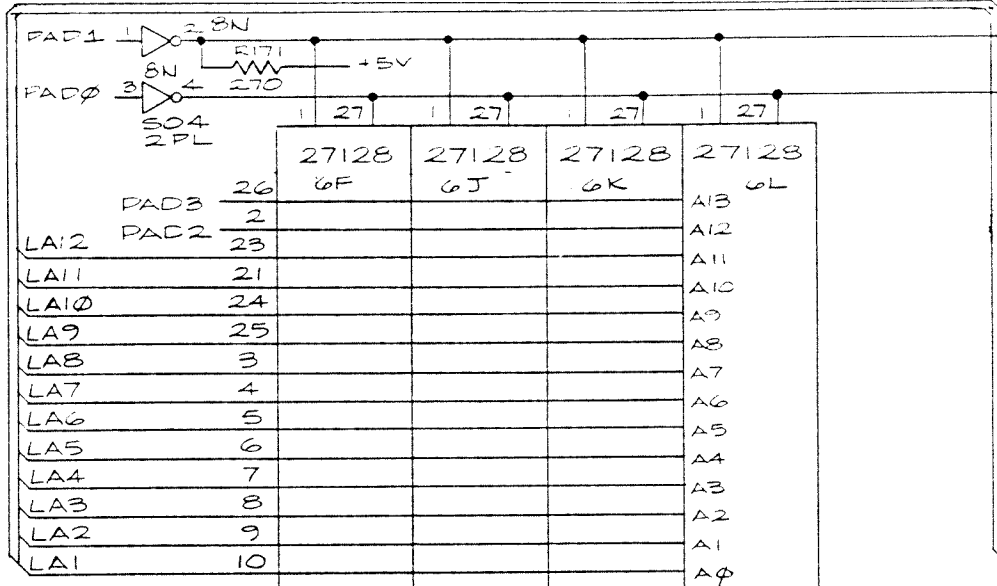
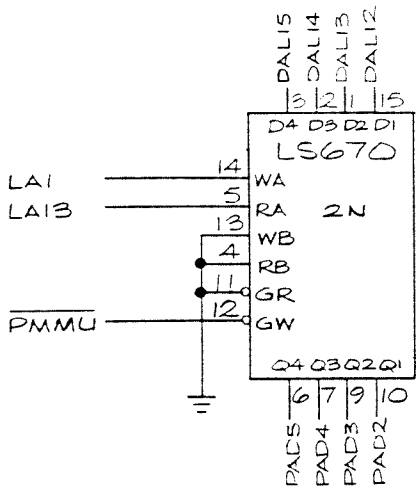
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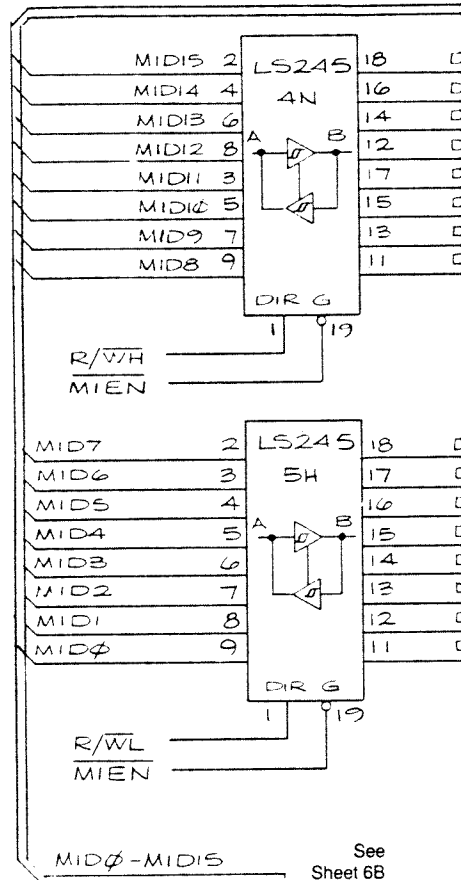
APB™ CPU PCB Schematic Diagram

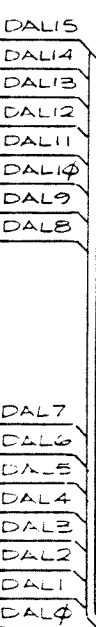
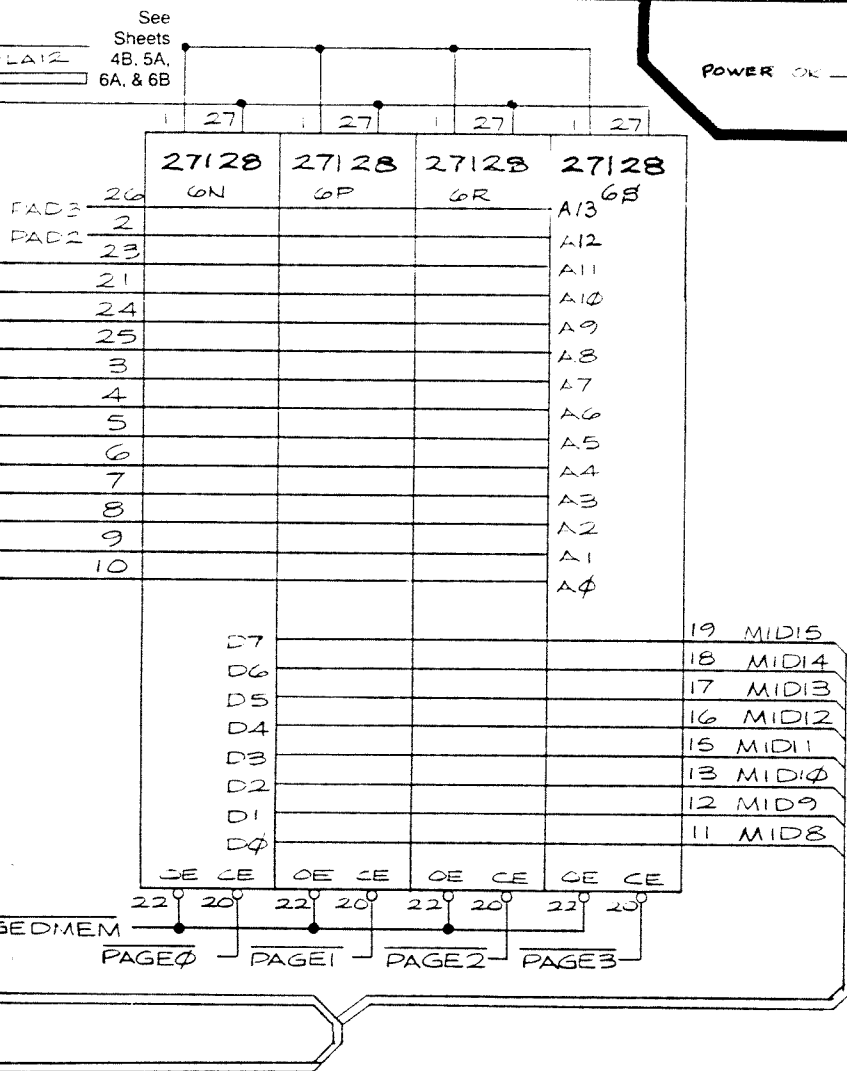
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SP-308 Sheet 5A 1st printing

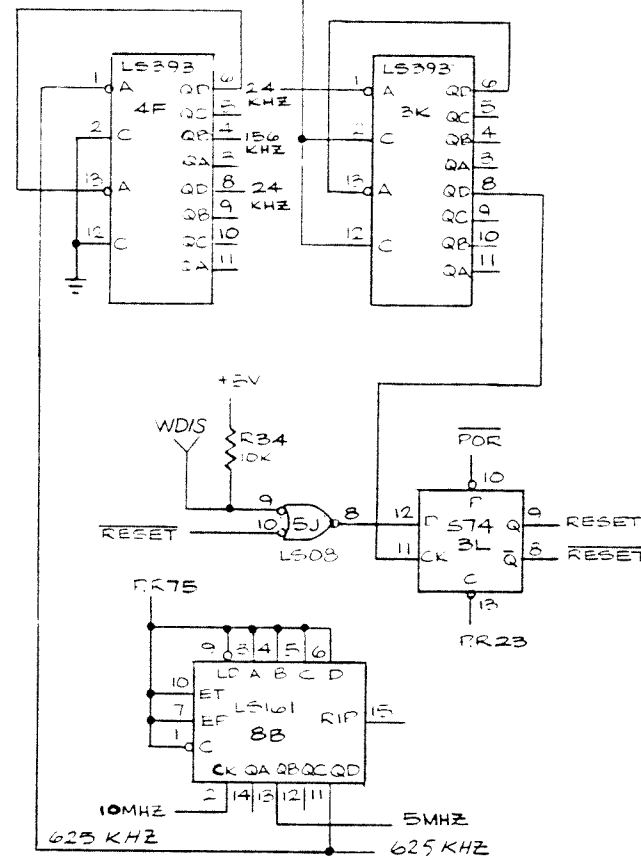
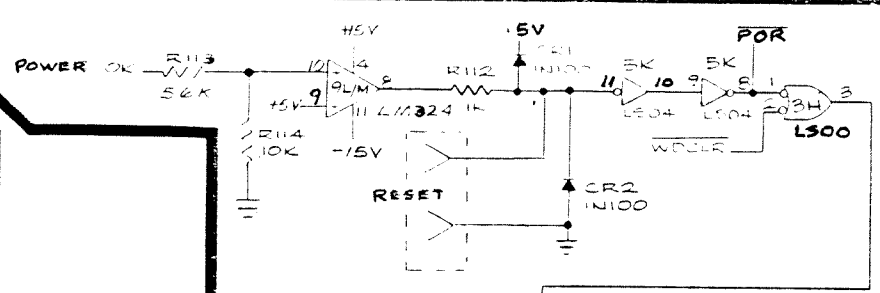


Paged Program ROM





See Sheets 4B, 6A, 6B, & 7B



Reset and Watchdog Clear

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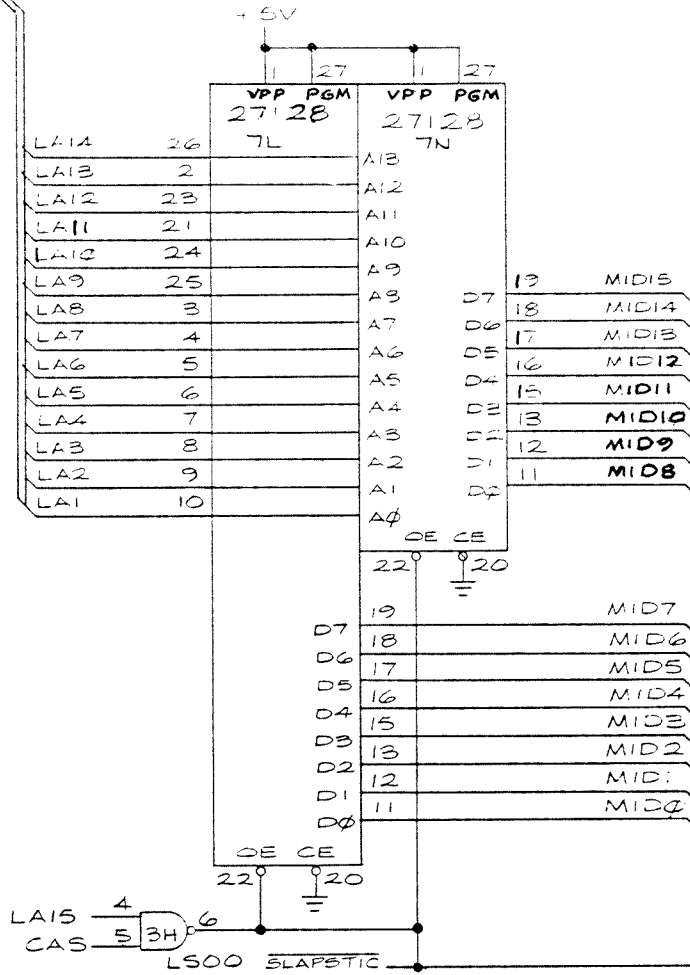
APB™ CPU PCB Schematic Diagram

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SP-308 Sheet 5B 1st printing

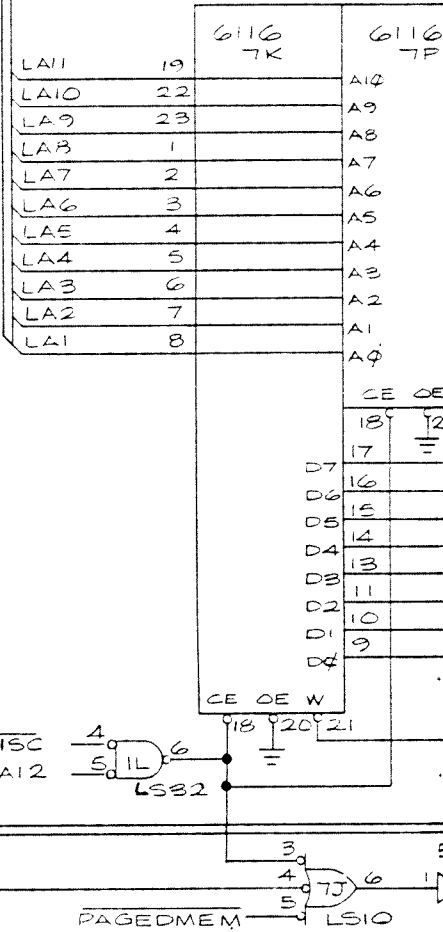
Fixed Program ROM

LA1 - LA14
See Sheet 5A & 5B



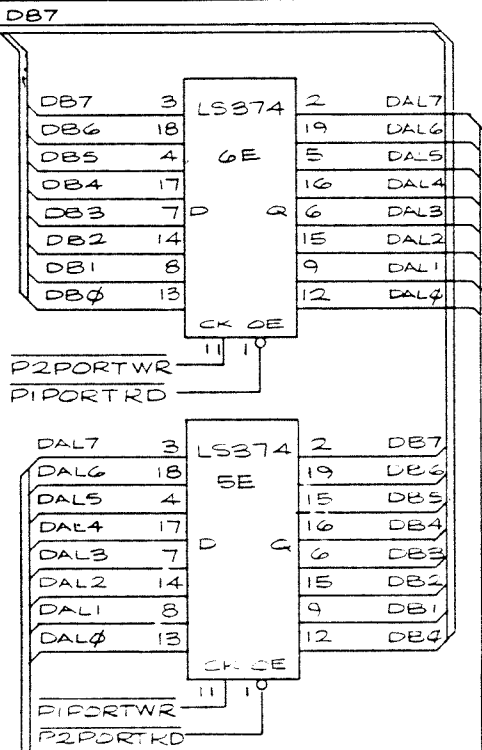
See Sheet 5B MID0 - MID15

Zero-Page RAM



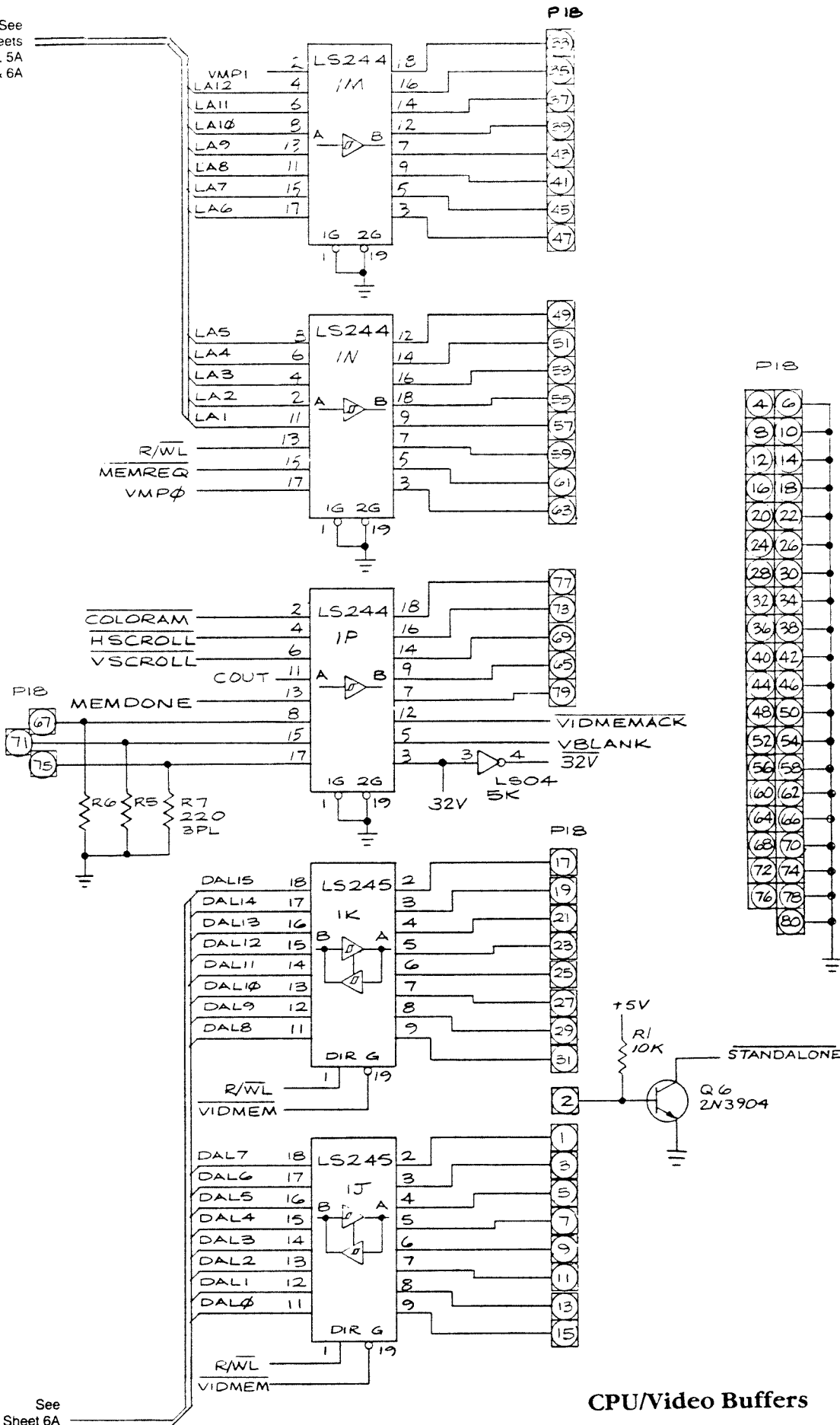
6502 Microprocessor Communication Latches

See Sheets 7A, 8A, & 8B



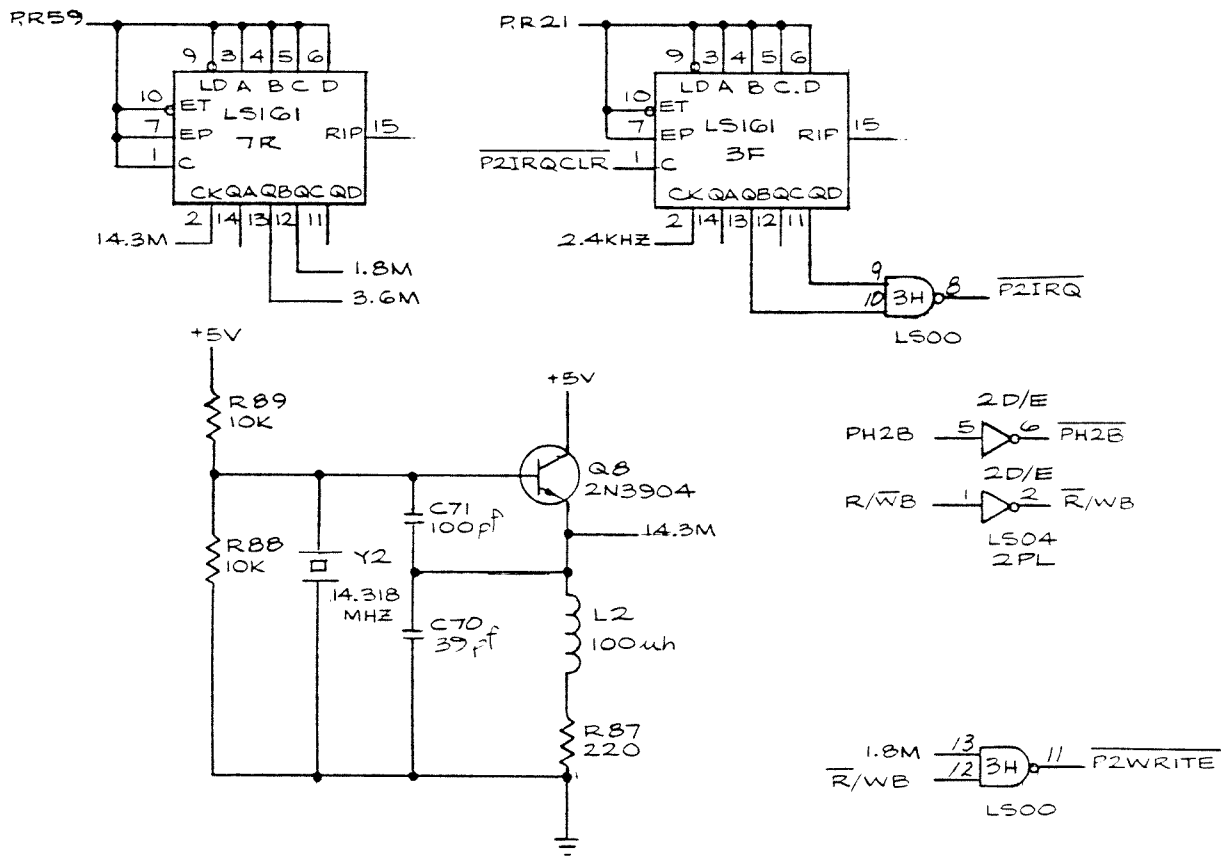
See Sheet 4B DAL0 - DAL15

See
Sheets
4B, 5A
& 6A



See
Sheet 6A

CPU/Video Buffers



Clock and Control Signals

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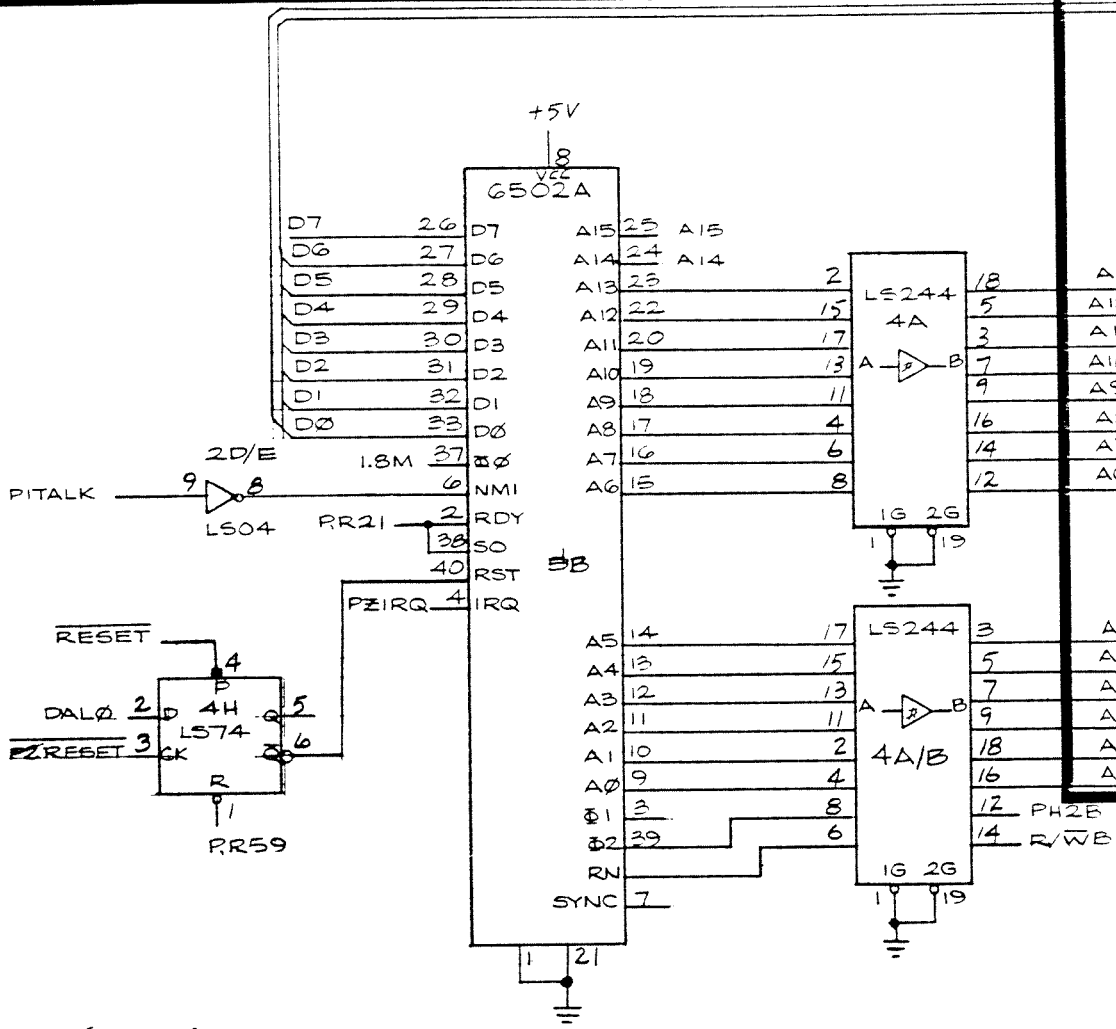
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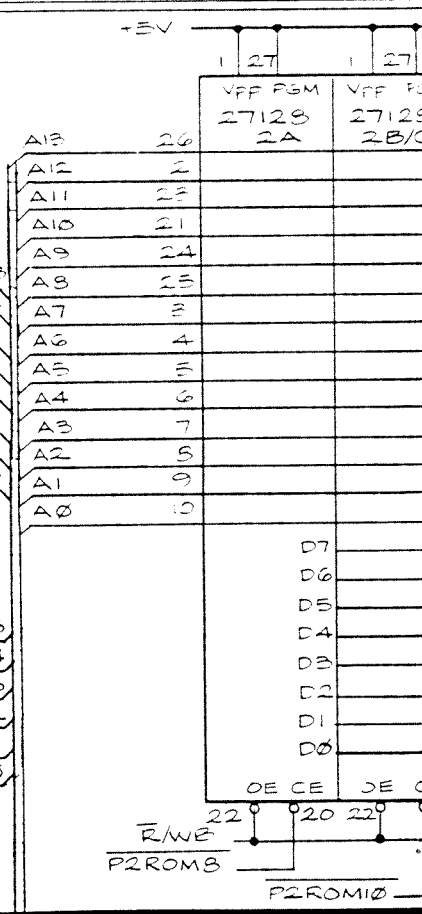
APB™ CPU PCB Schematic Diagram

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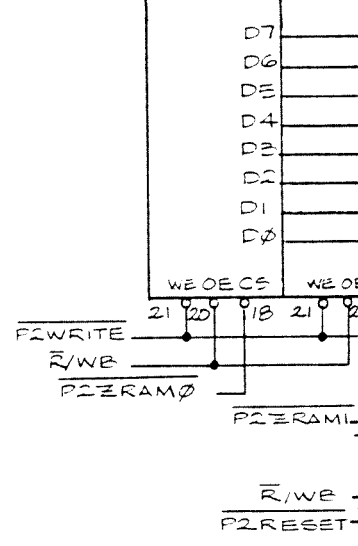
SP-308 Sheet 6B
1st printing



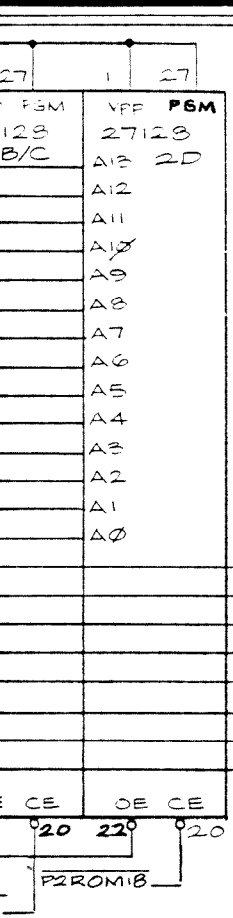
6502 Microprocessor



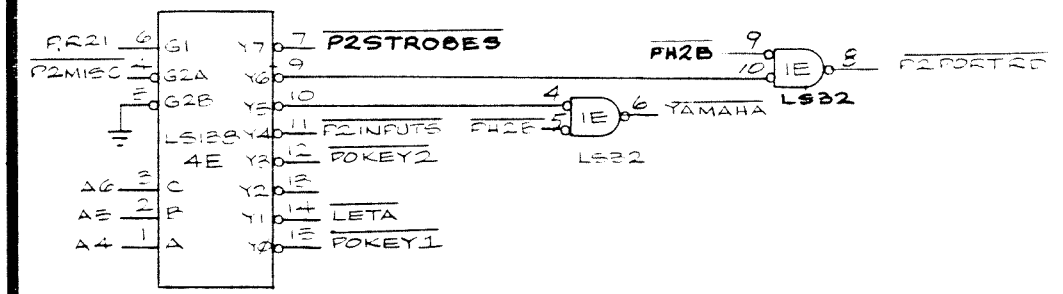
Pin	Signal	6116 1A	6116 18/C
19	A10		
22	A9		
23	A8		
1	A7		
2	A6		
3	A5		
4	A4		
5	A3		
6	A2		
7	A1		
8	A0		



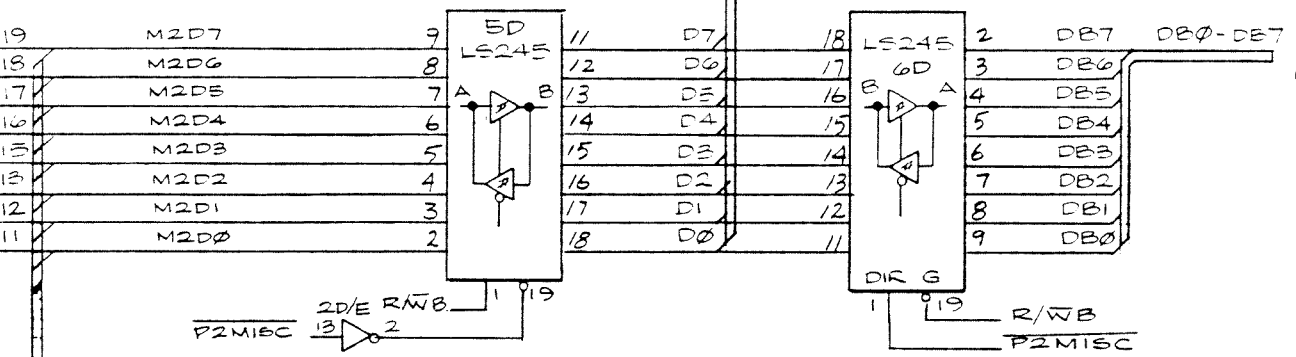
P2RAM1



Address Decoding

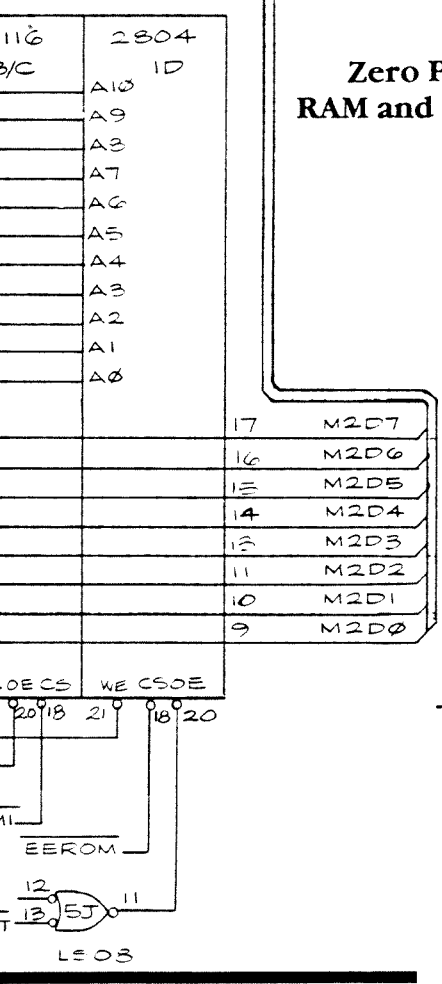


Program Memory



See Sheets 6A, 8A, & 8B

Zero Page RAM and EEROM



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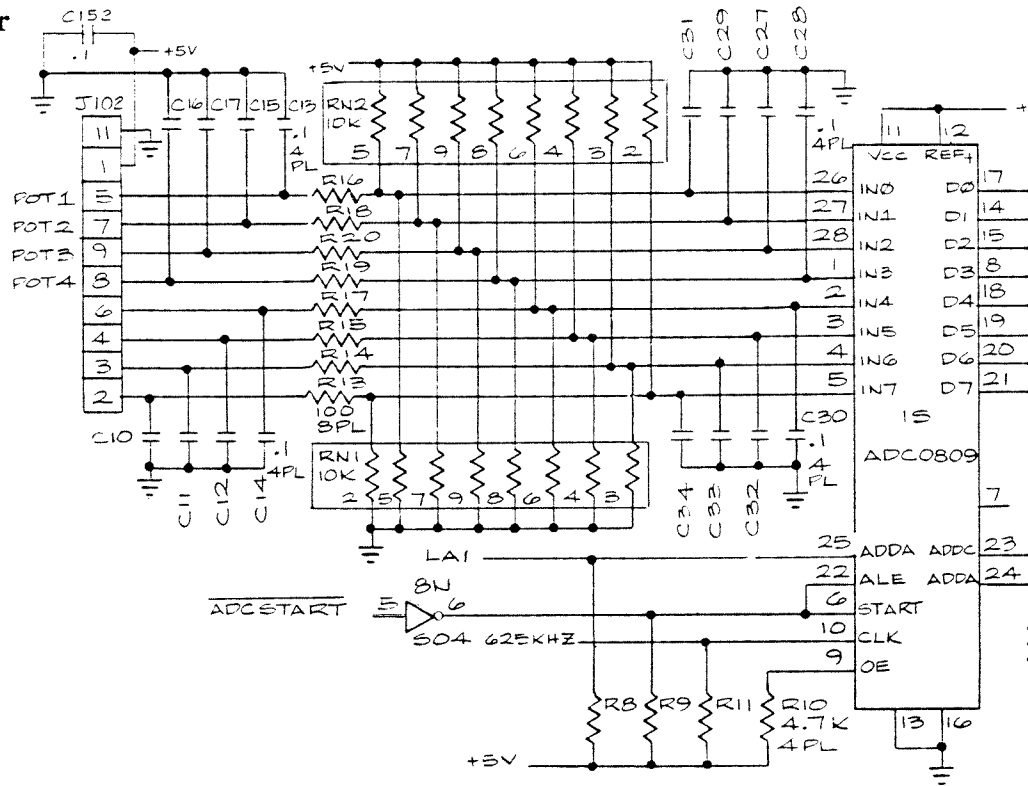


APB™ CPU PCB Schematic Diagram

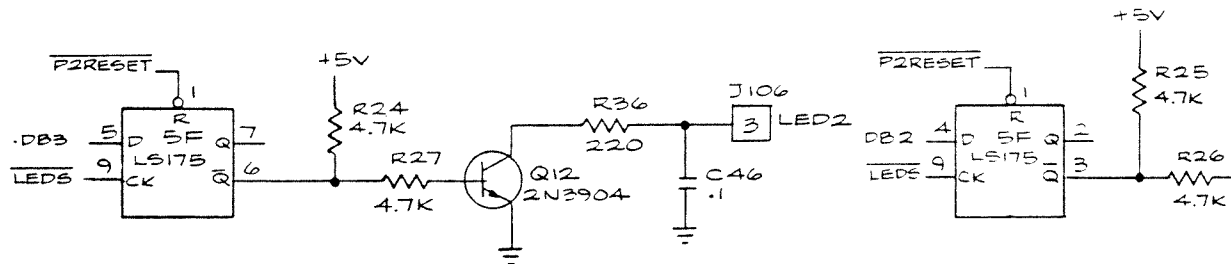
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SP-308 Sheet 7A
1st printing

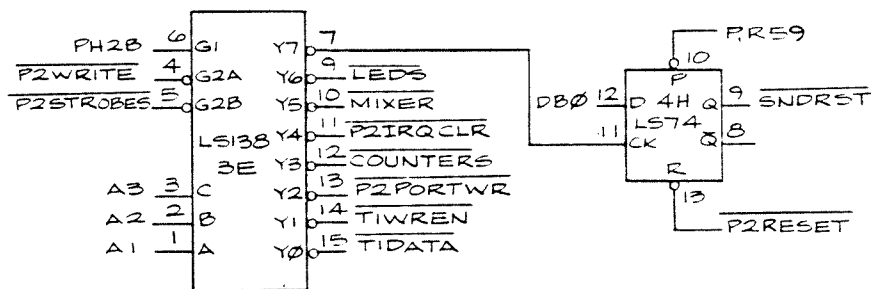
A/D Converter

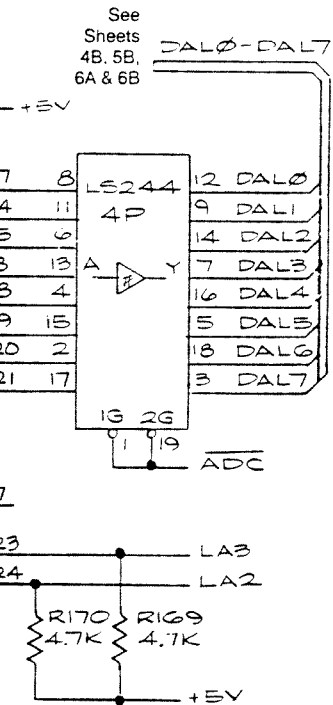


LED Drivers

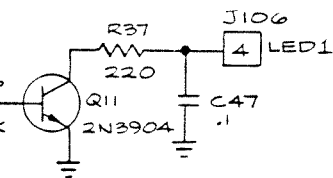
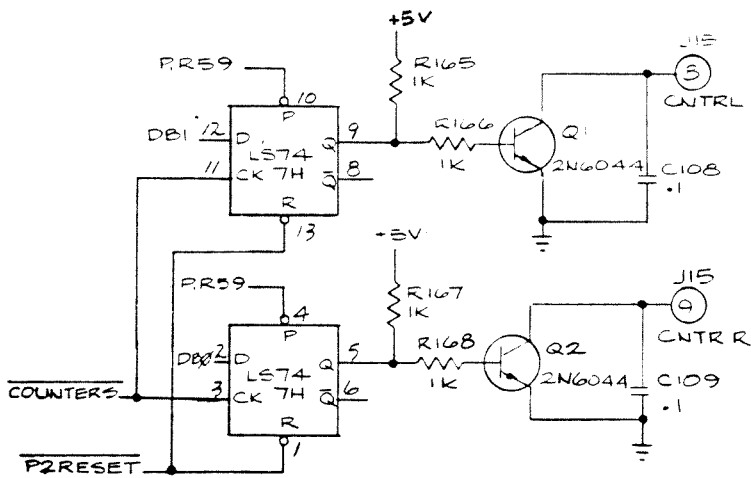


Address Decoding

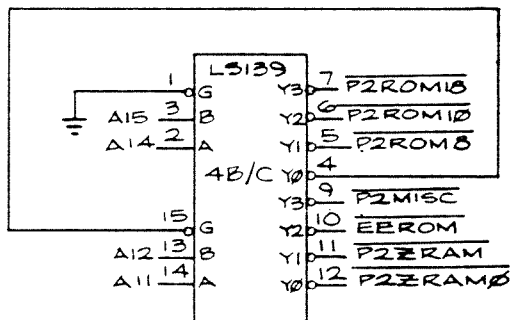




Coin Counters



Address Decoding



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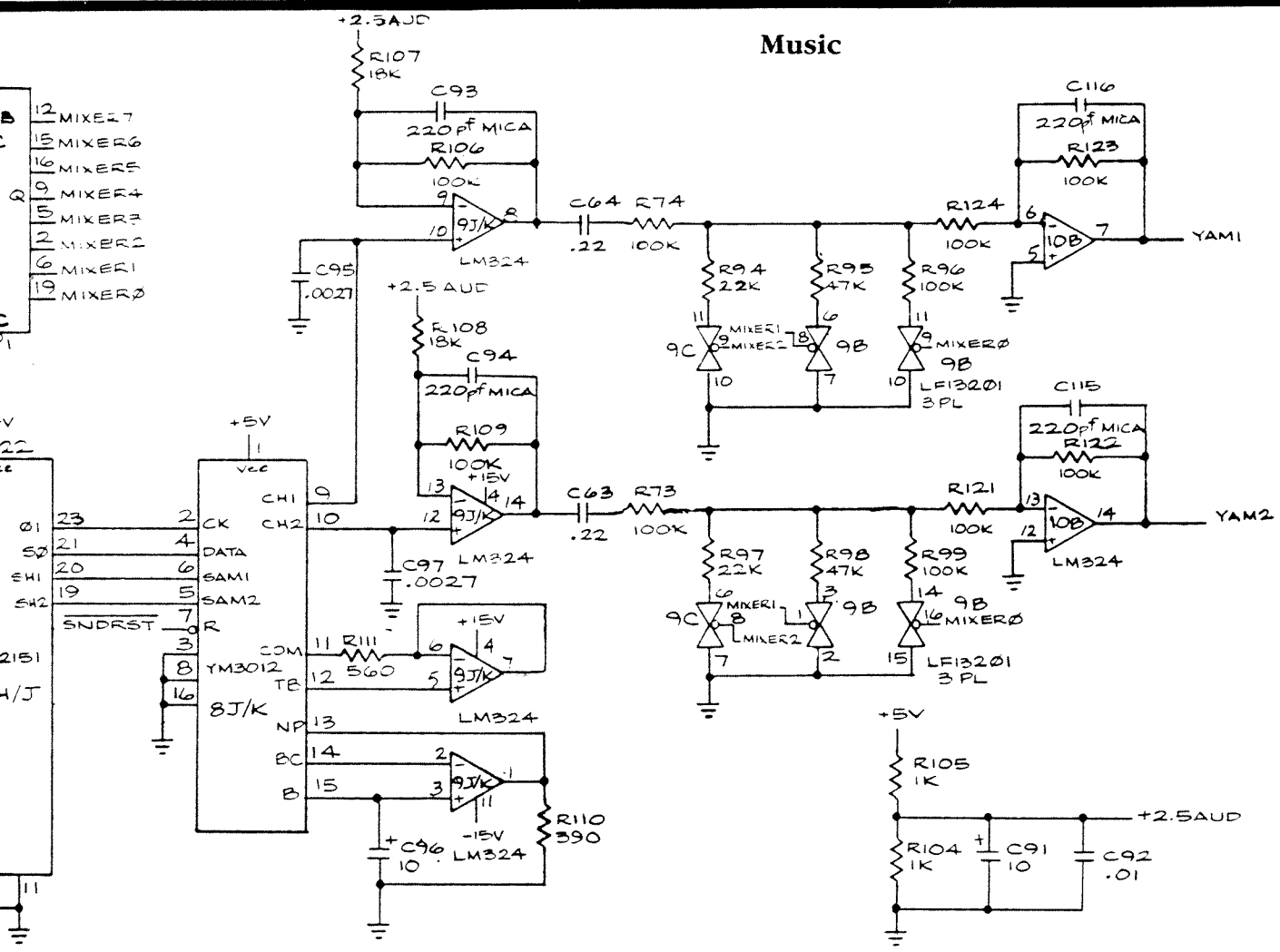
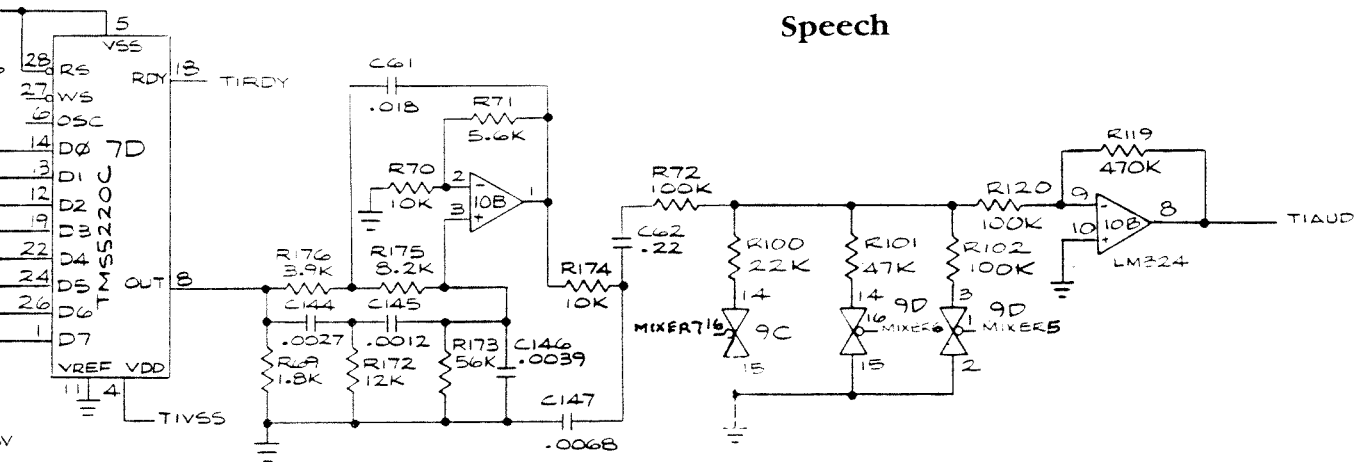
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APB™ CPU PCB Schematic Diagram

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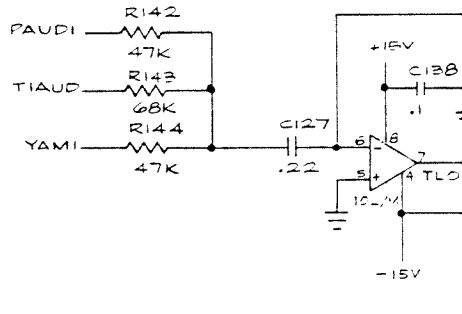
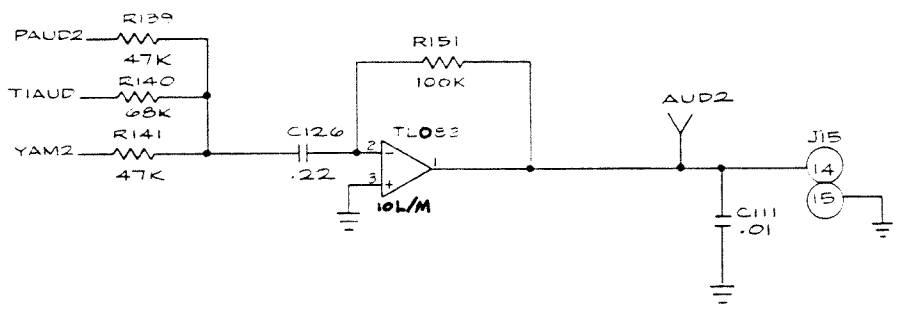
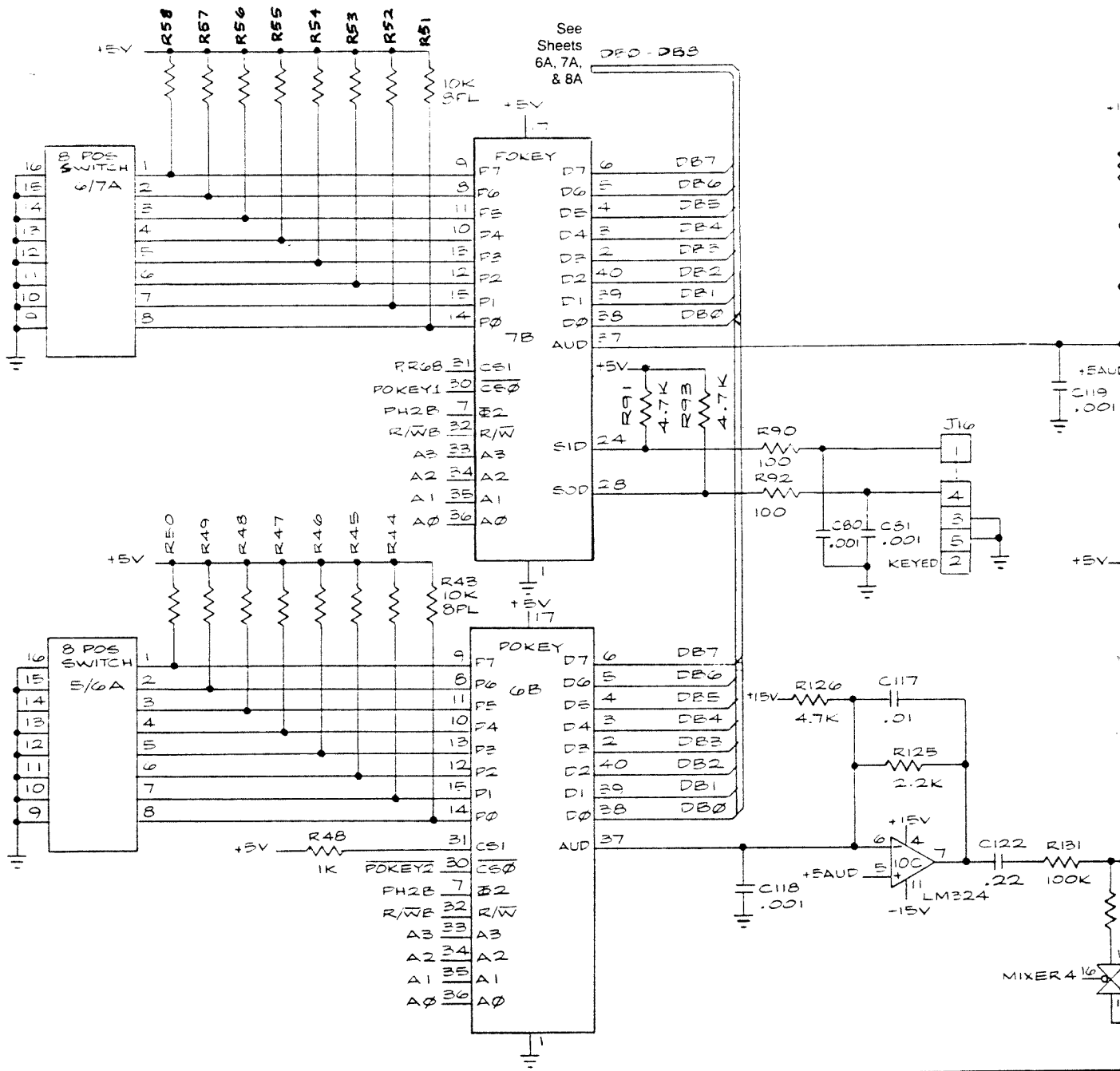
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**APB™ CPU PCB
Schematic Diagram**

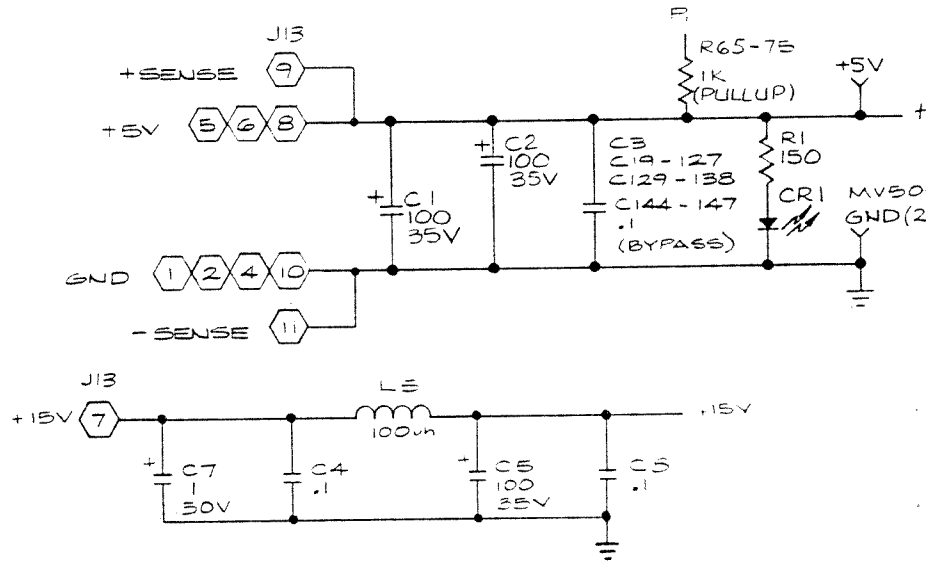
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SP-308 Sheet 8A
1st printing



Audio Output Dr

Power In

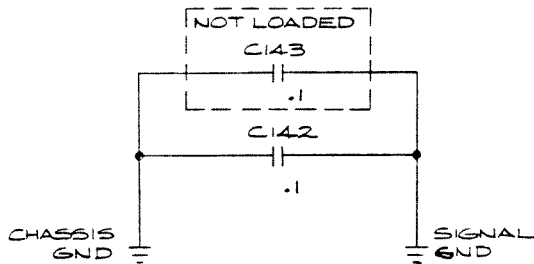


Power Input

+5V

VBOE3
D(2)

- DESIGNATES CONNECTOR J18
- ⬡ DESIGNATES CONNECTOR J13
- DESIGNATES CONNECTOR J19



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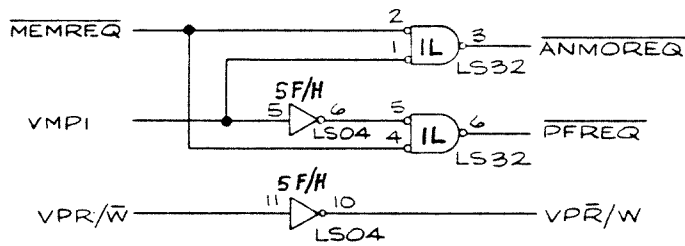
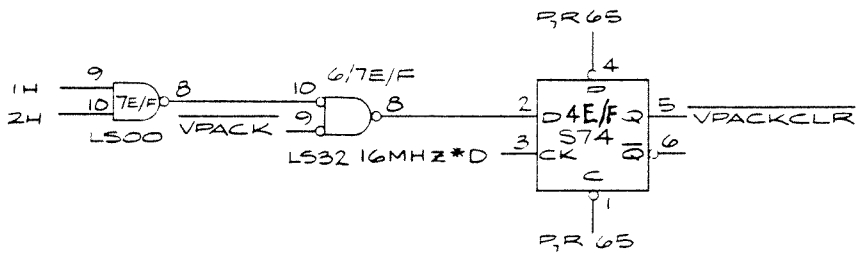
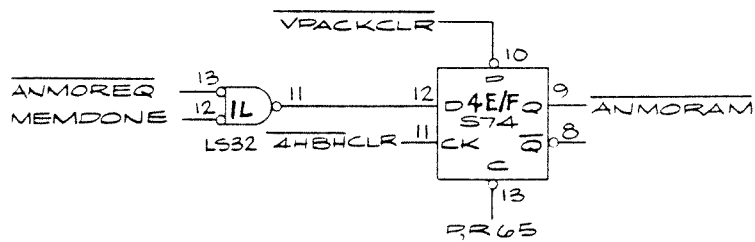
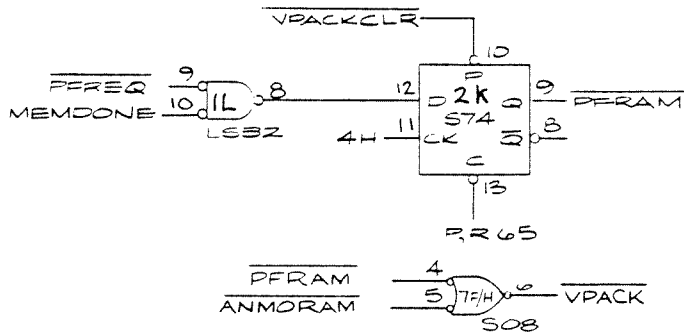
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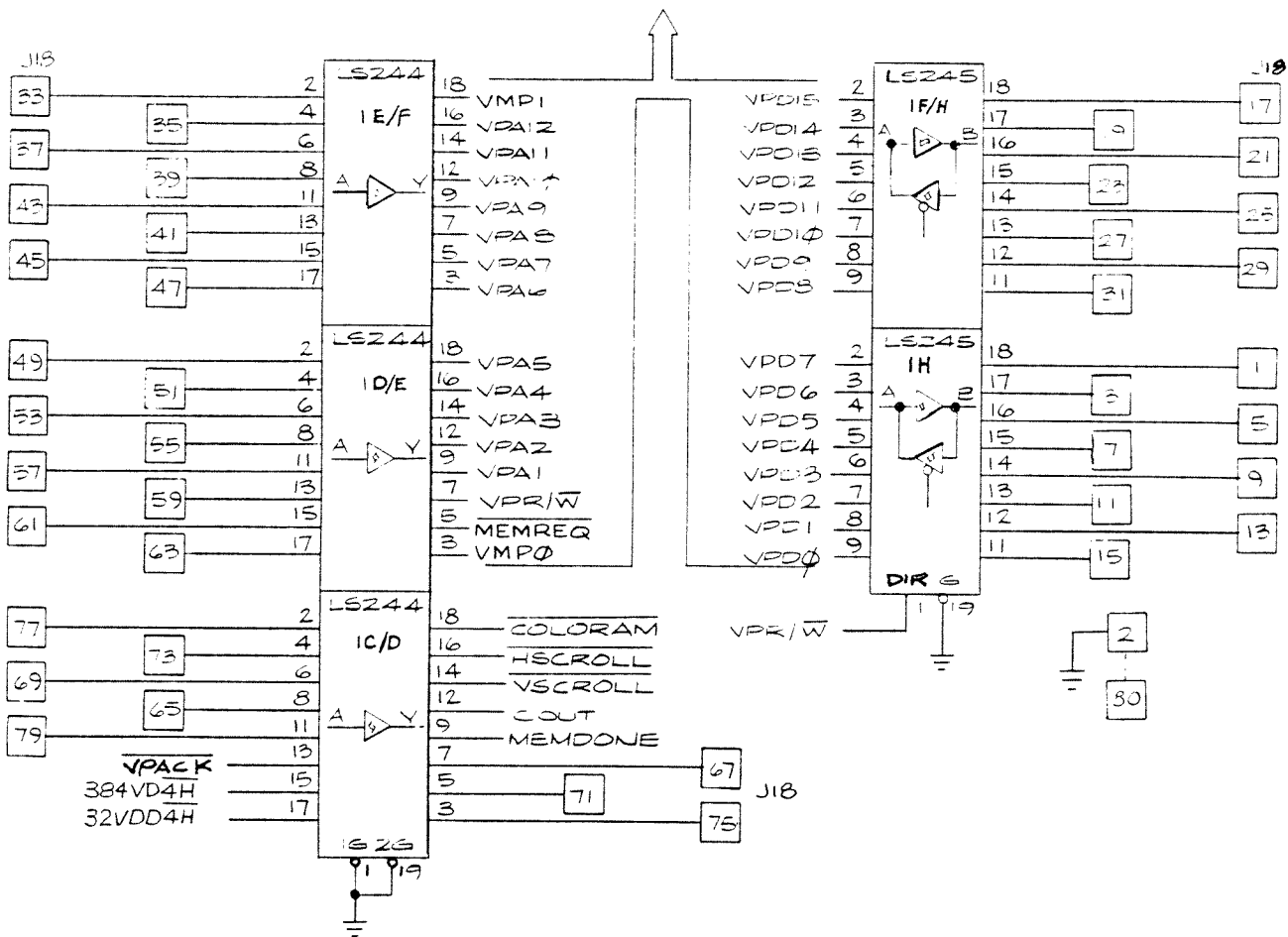
**APB™ Video PCB
Schematic Diagram**

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**SP-308 Sheet 9A
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Address Decoding Control Signals



Video/CPU Buffers

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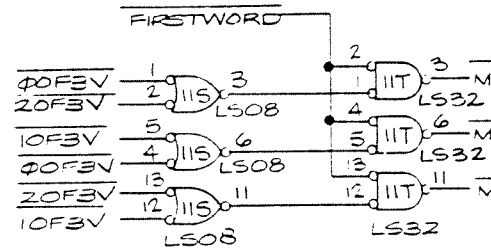
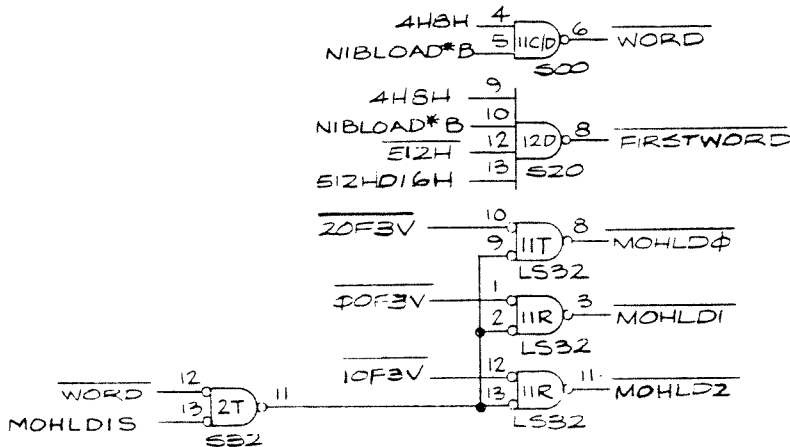
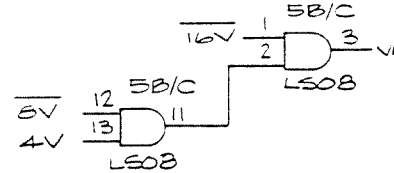
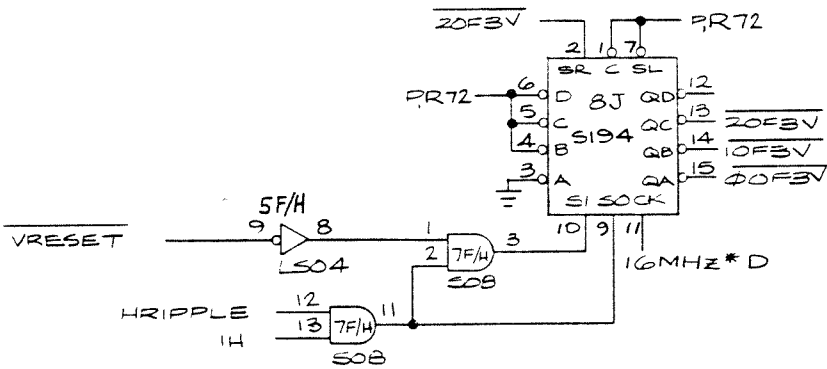
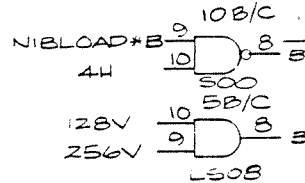
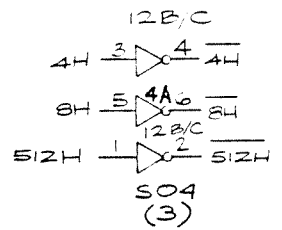
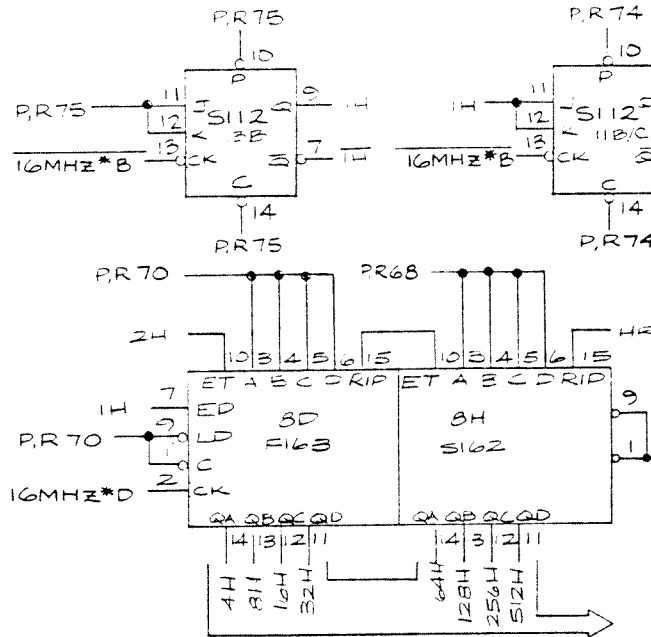
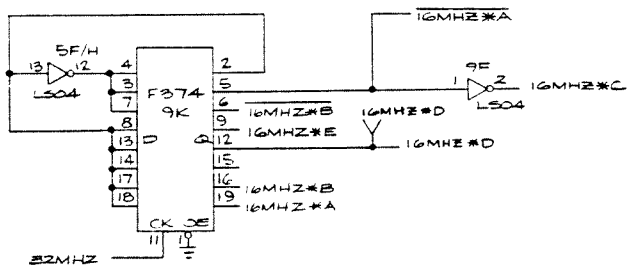
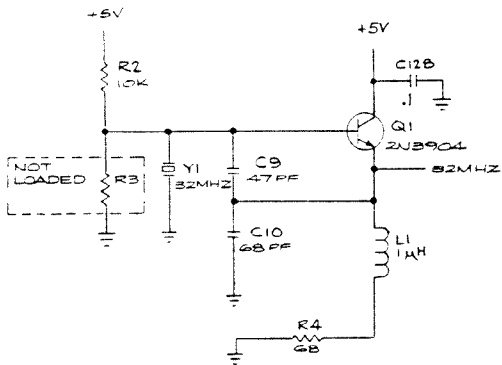


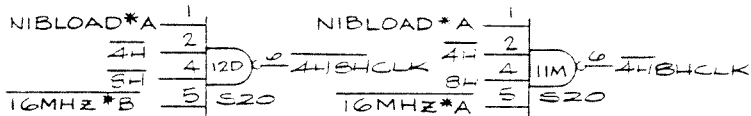
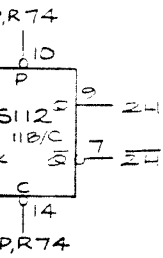
**APB™ Video PCB
Schematic Diagram**

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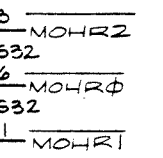
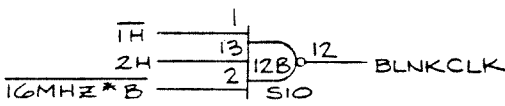
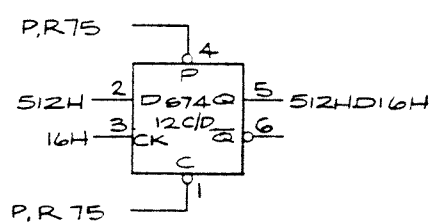
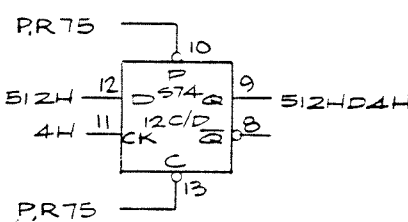
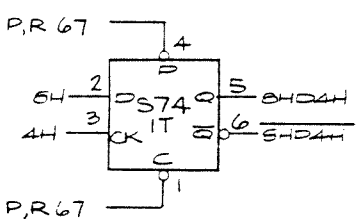
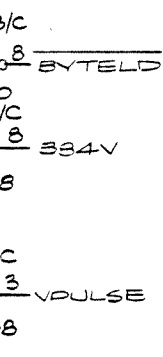
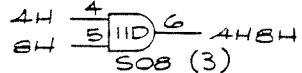
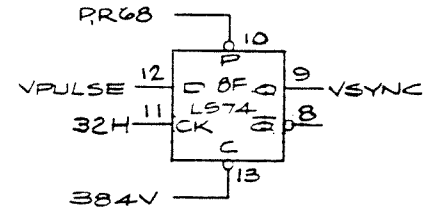
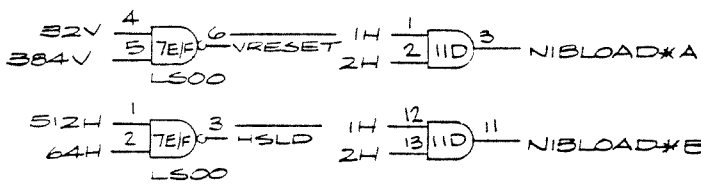
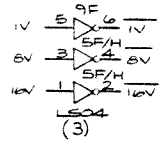
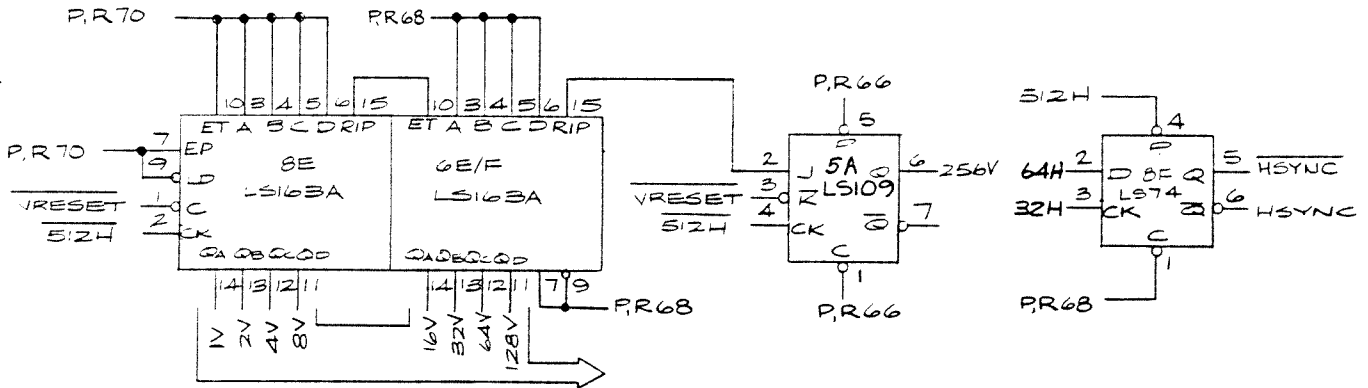
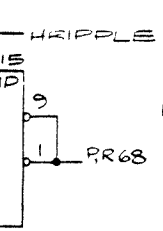
SP-308 Sheet 9B
1st printing

Video Clock





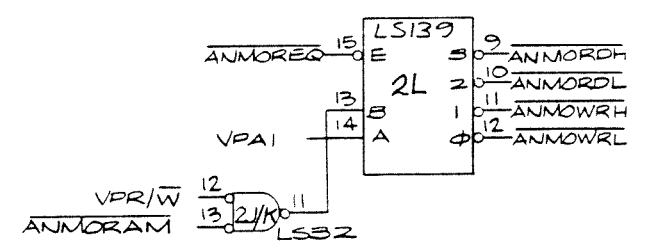
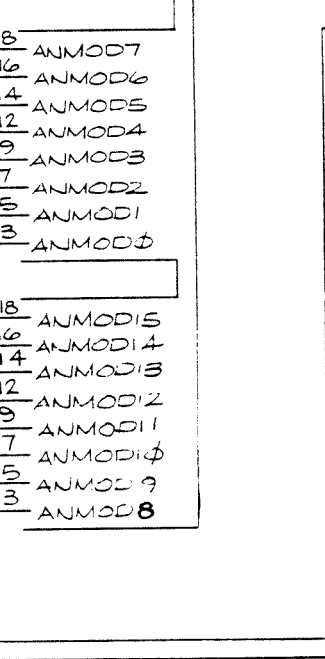
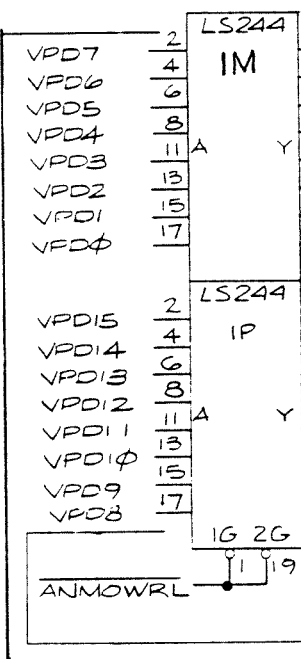
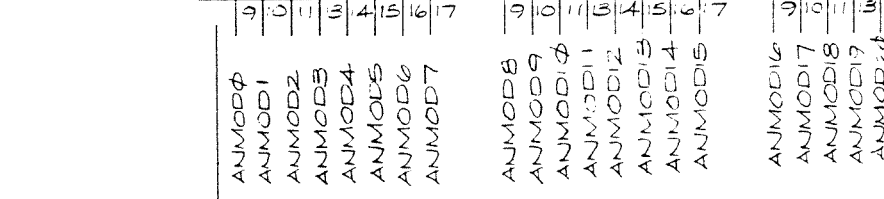
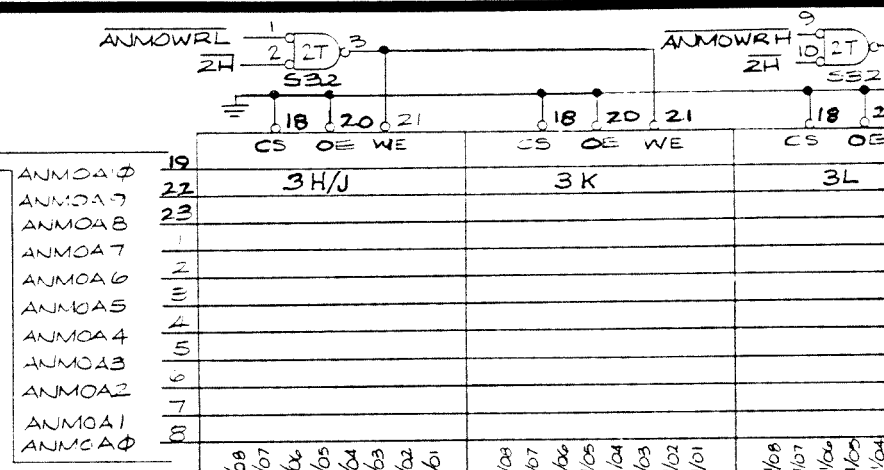
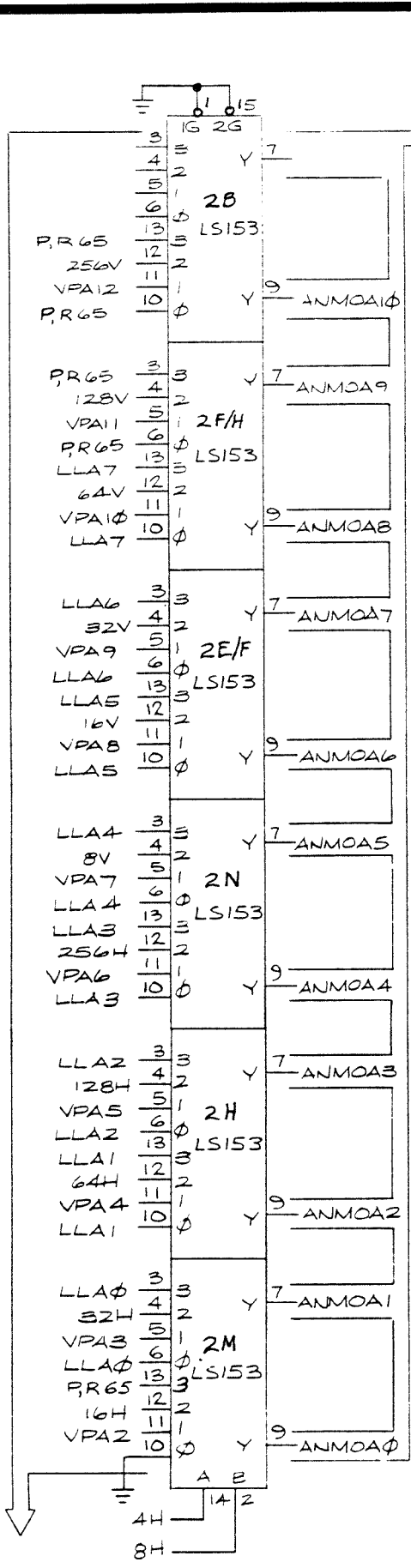
Sync Chain and Timing Strobes

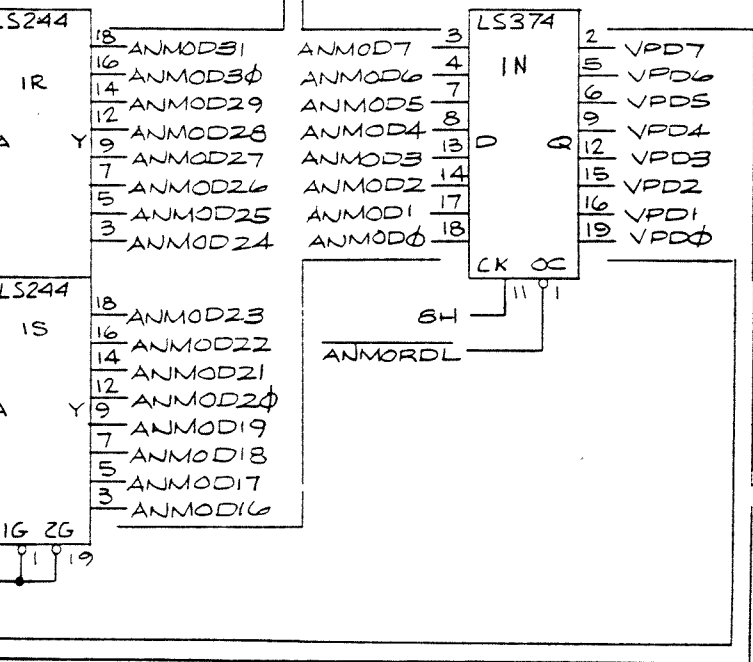
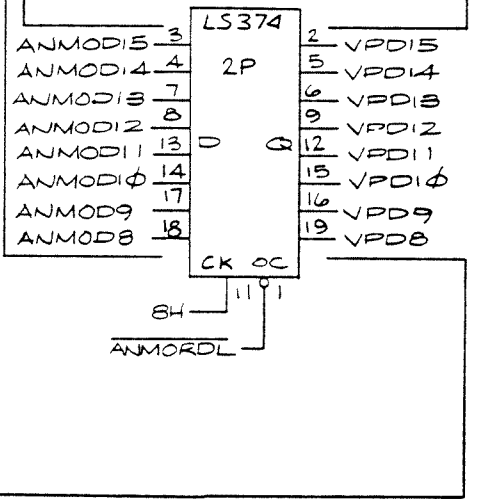
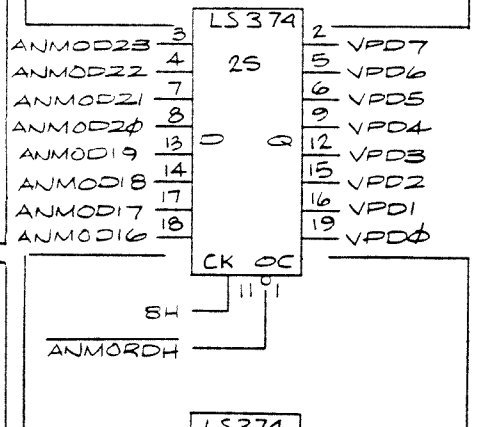
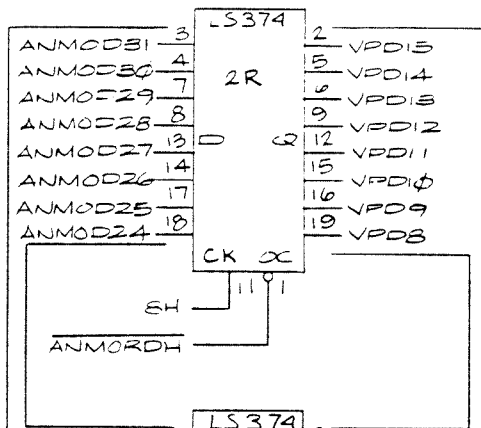
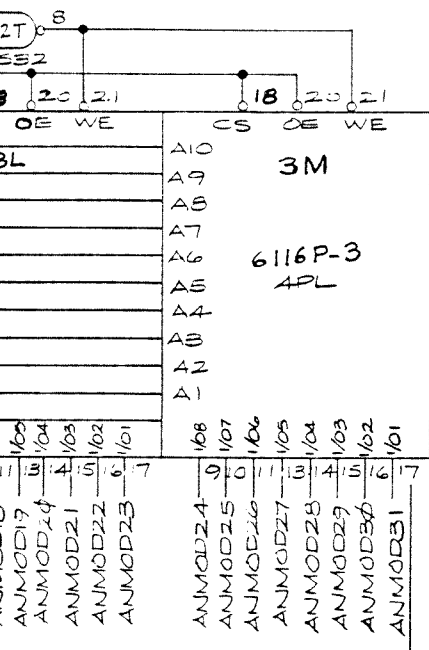


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APB™ Video PCB Schematic Diagram





Alphanumeric/Motion Object RAM

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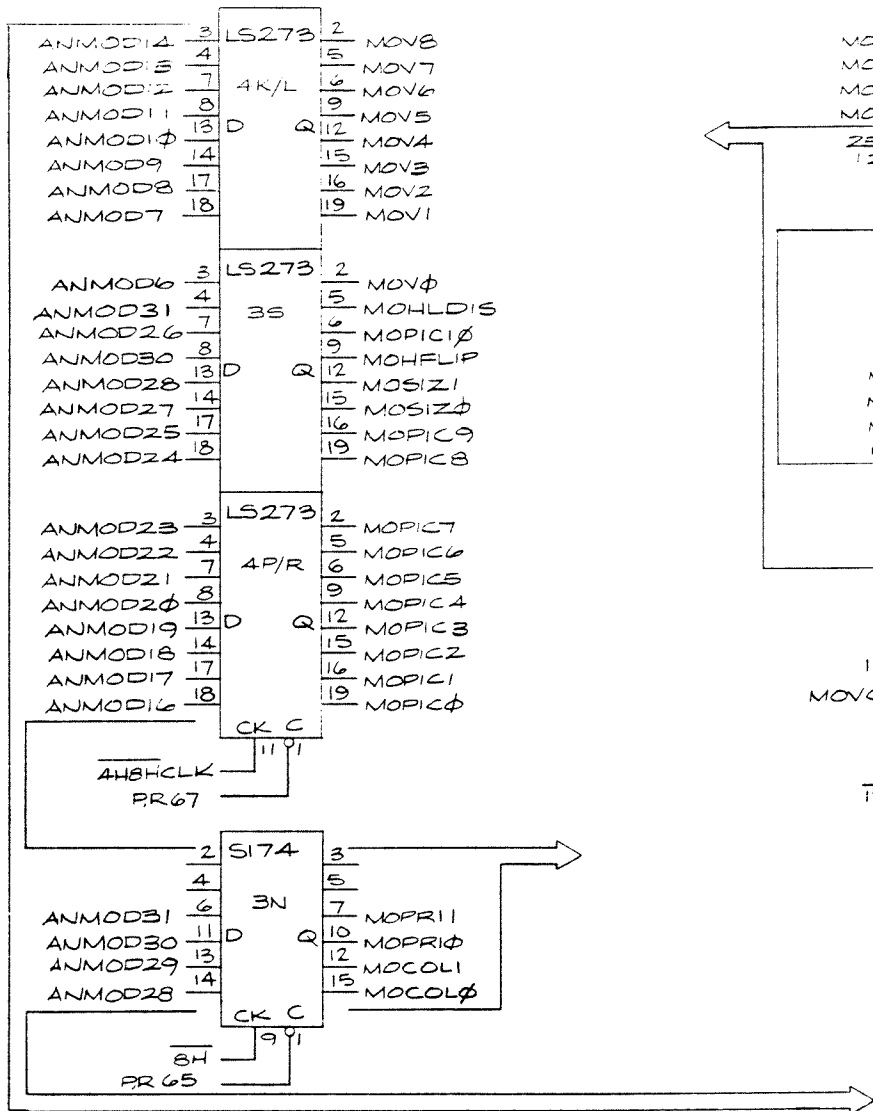
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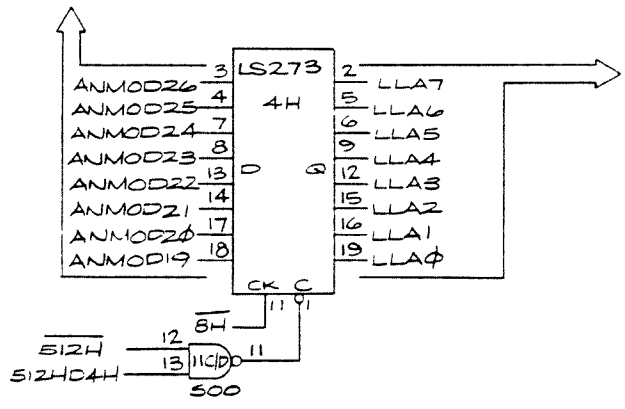
APB™ Video PCB Schematic Diagram

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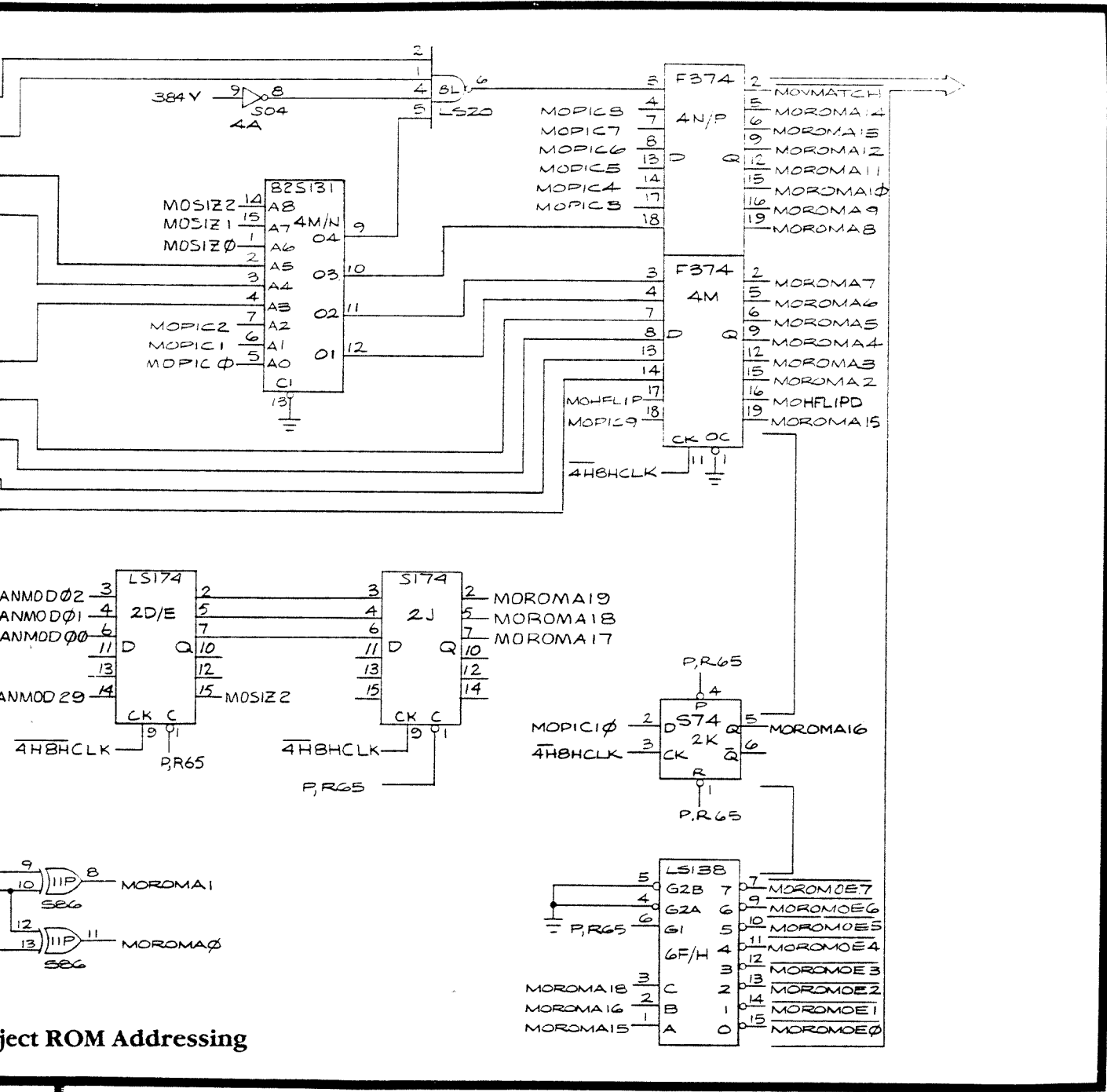
SP-308 Sheet 10B
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Motion Object



Link List Address Latch



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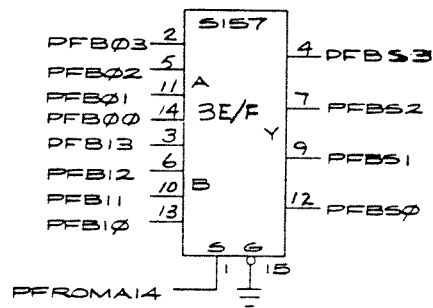
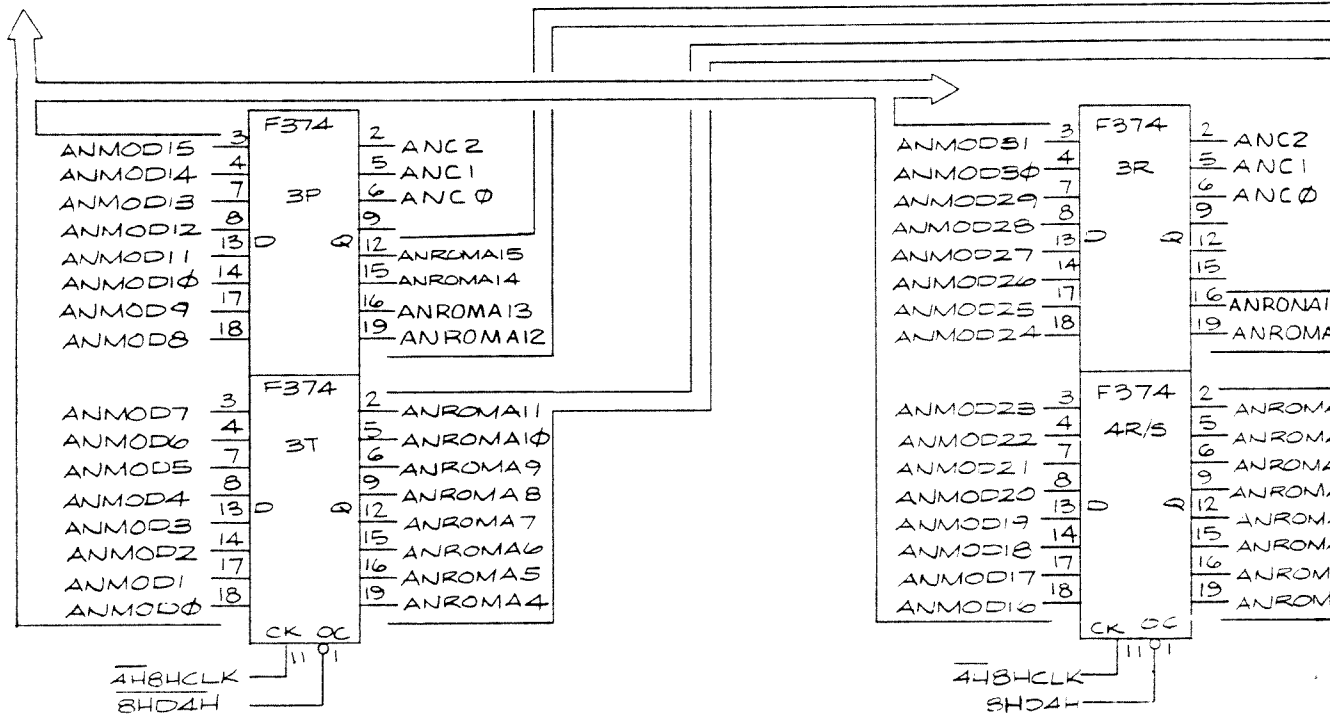


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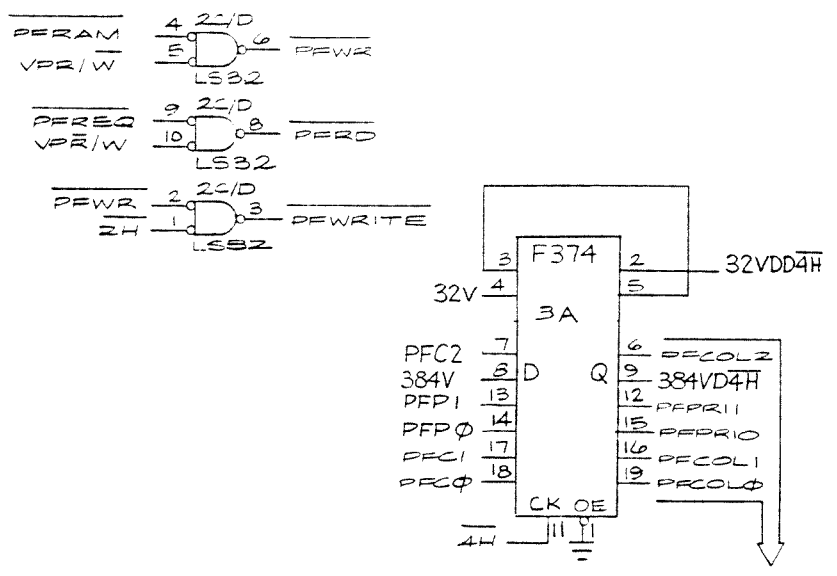
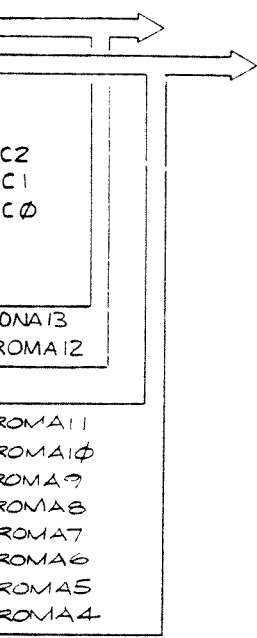
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Alphanumeric ROM Addressing



Playfield Bank Select



Playfield Data Latch Strobes

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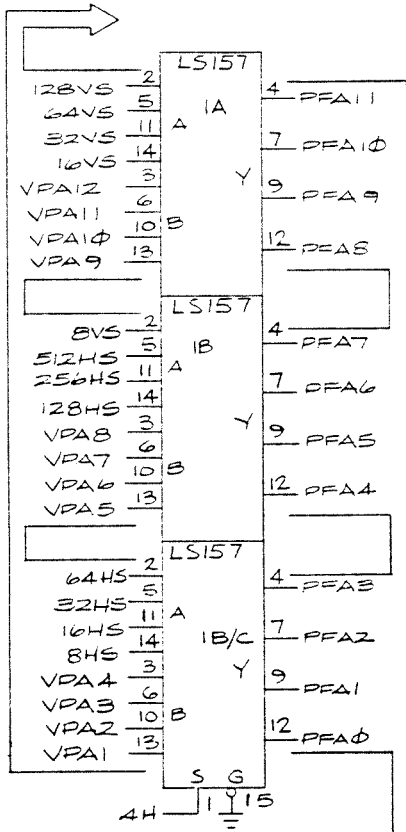
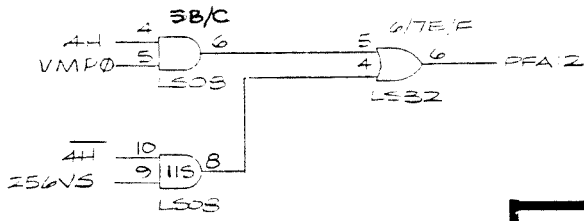


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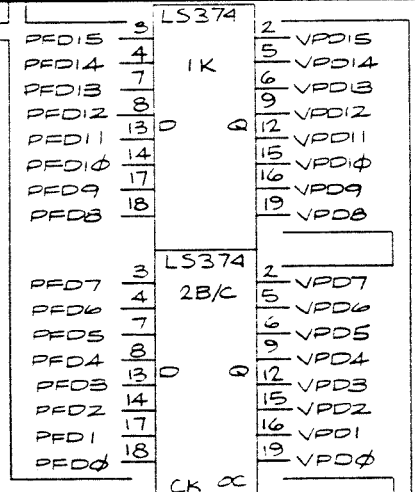
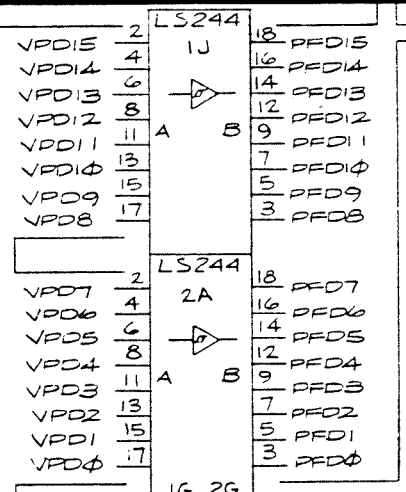
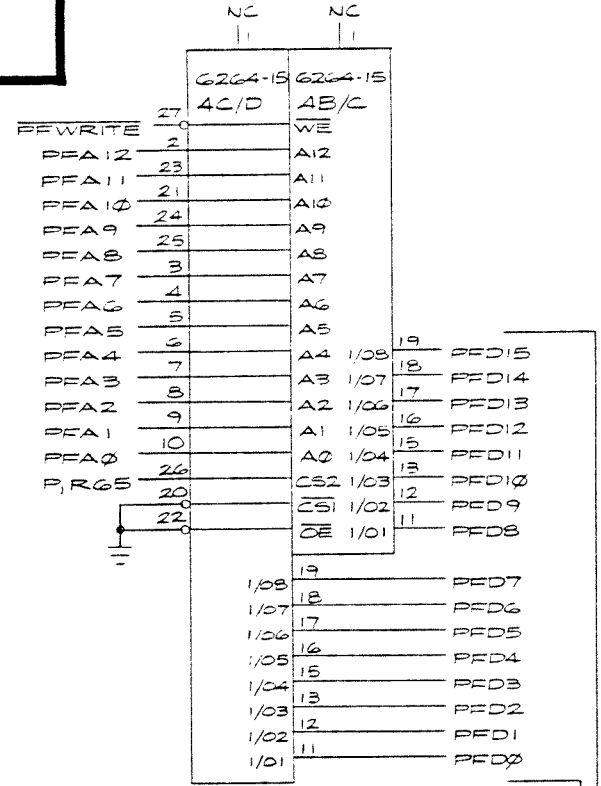
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Playfield RAM Addressing

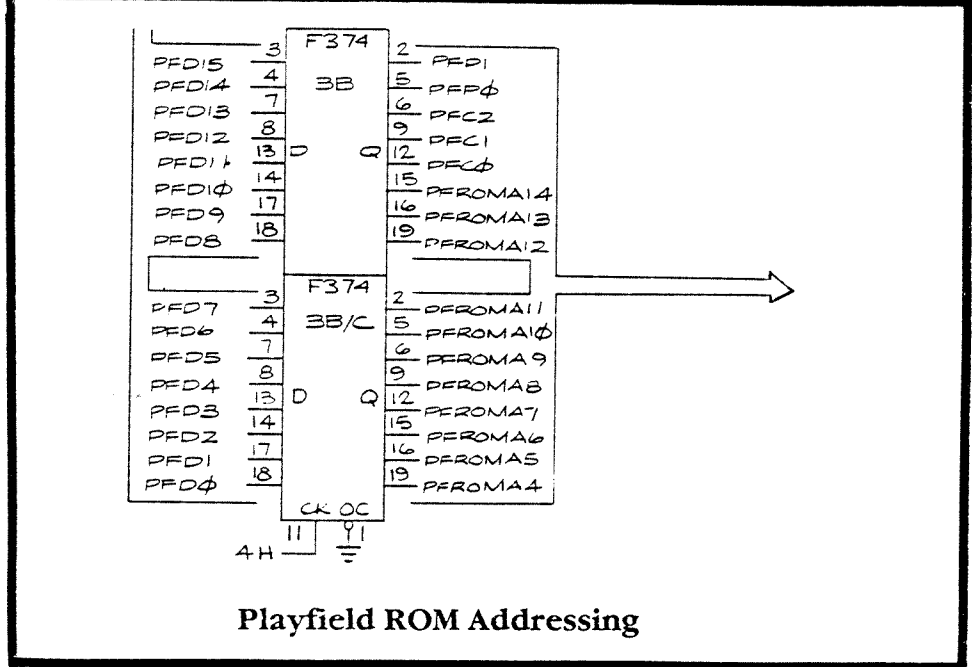
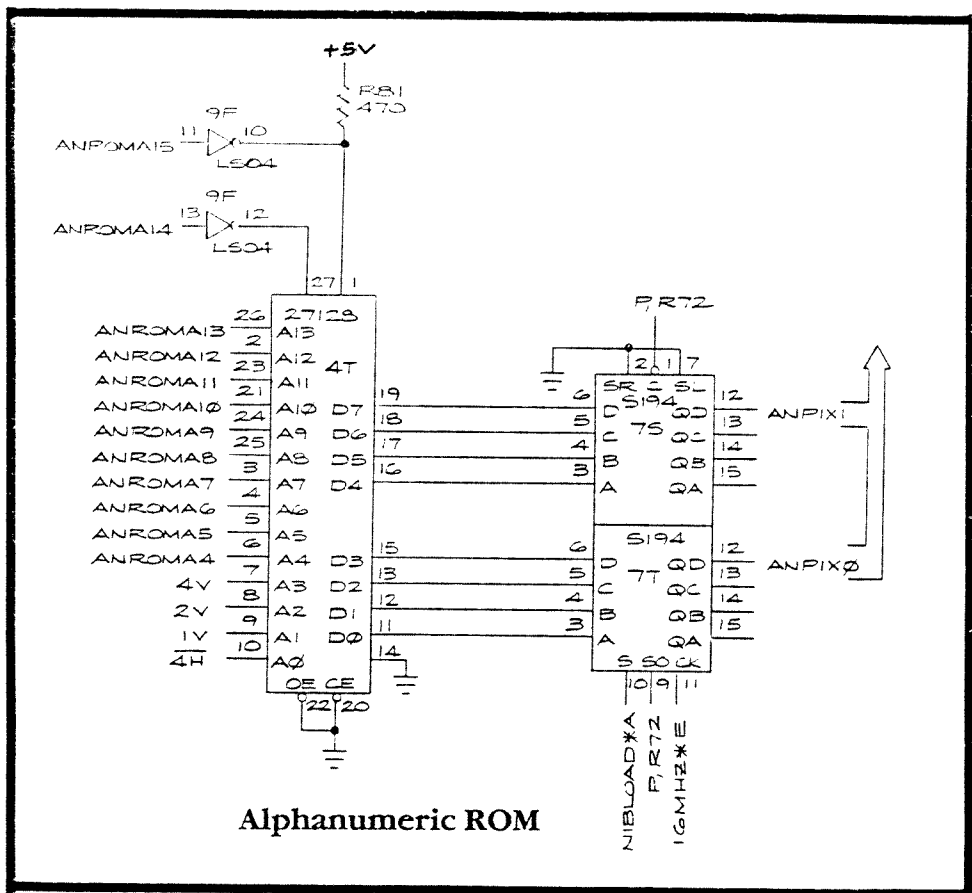


Playfield RAM



Playfield RAM Data Latches

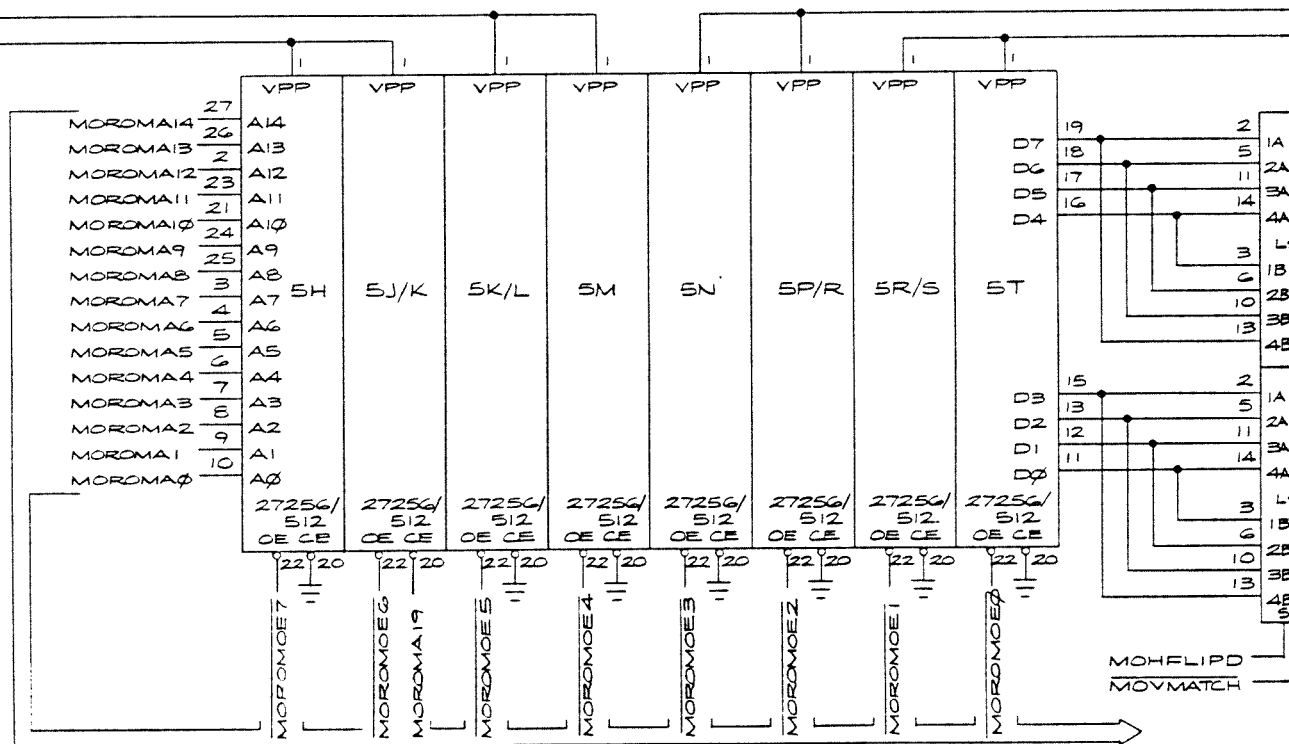
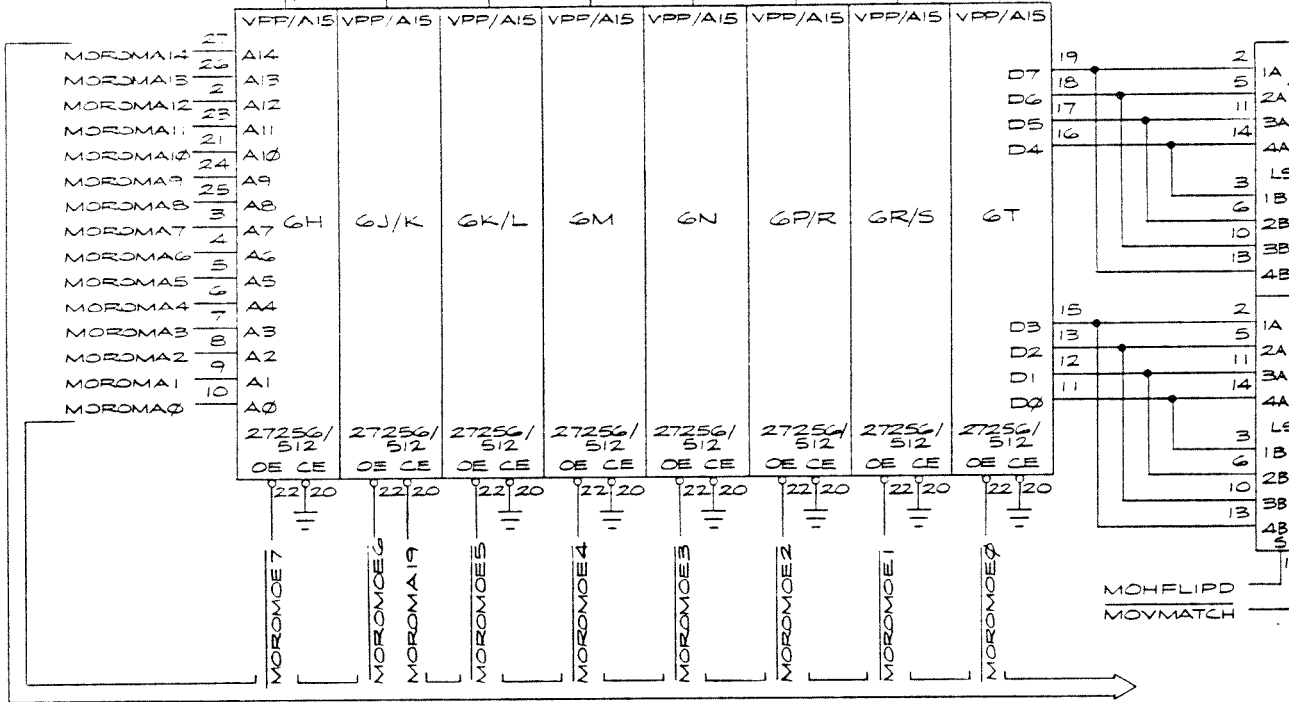
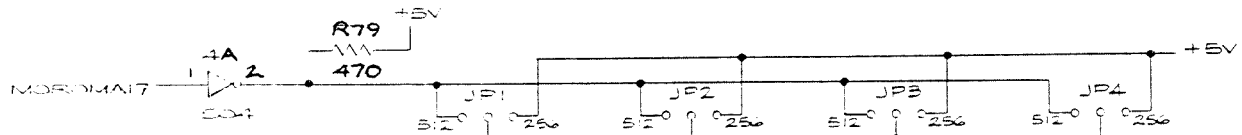




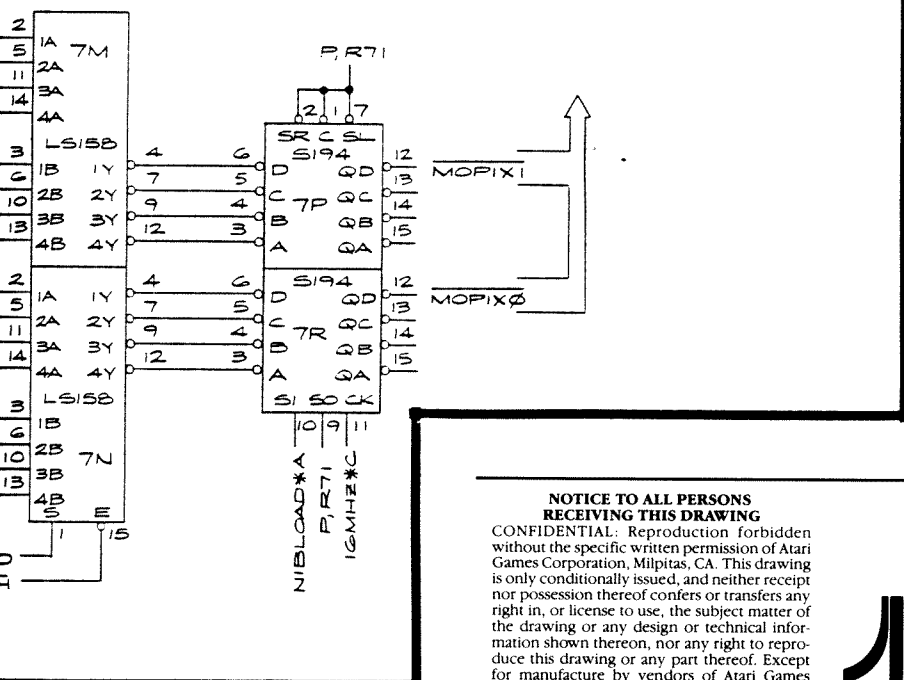
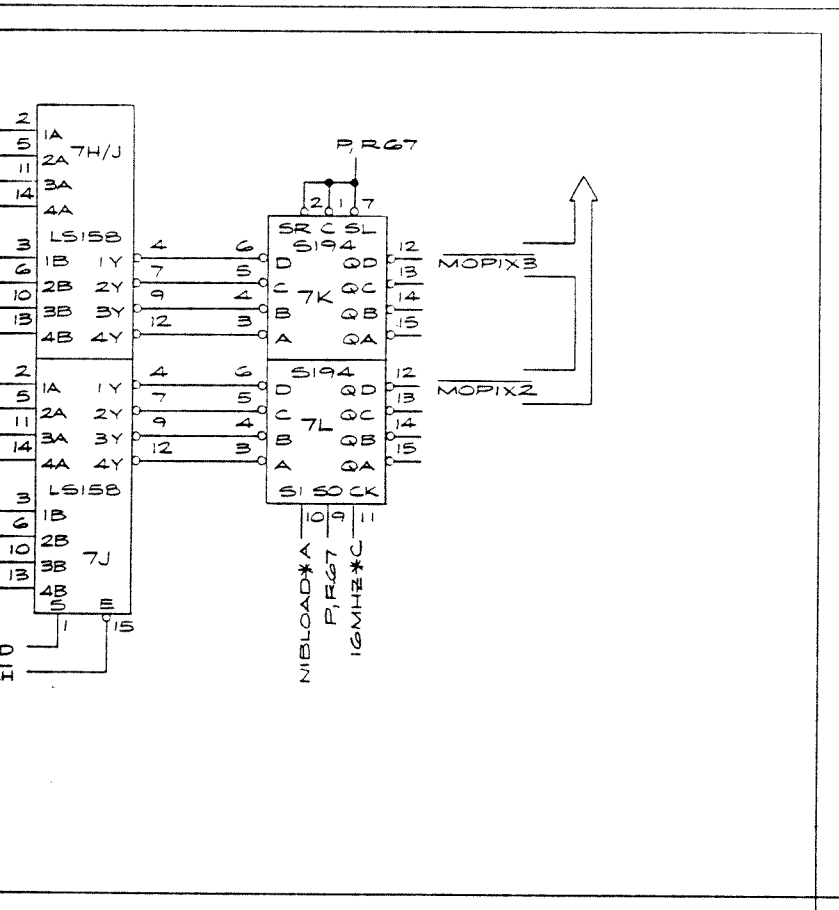
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Motion Object ROM

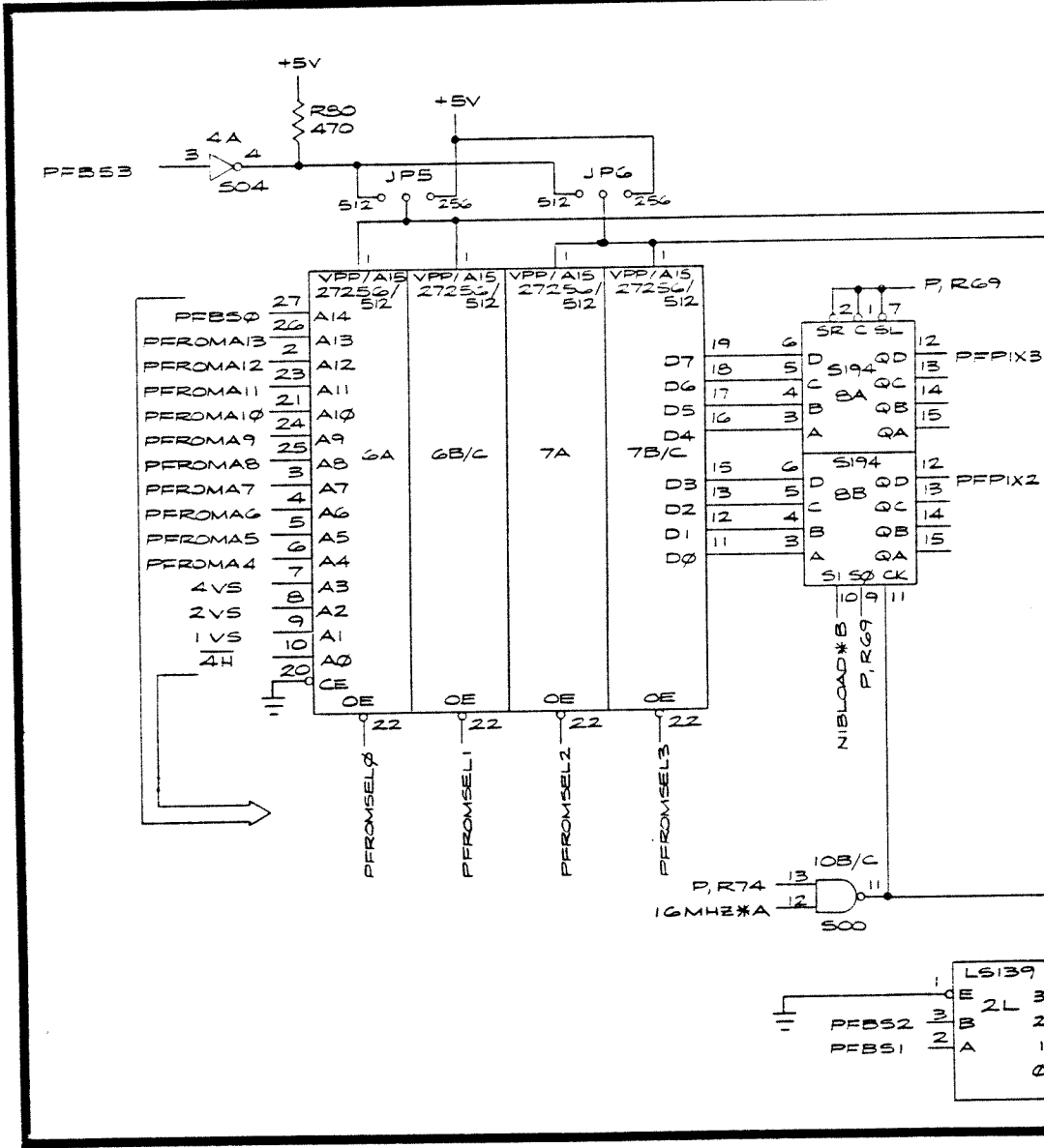


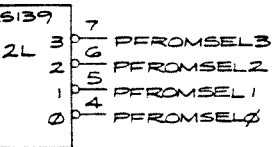
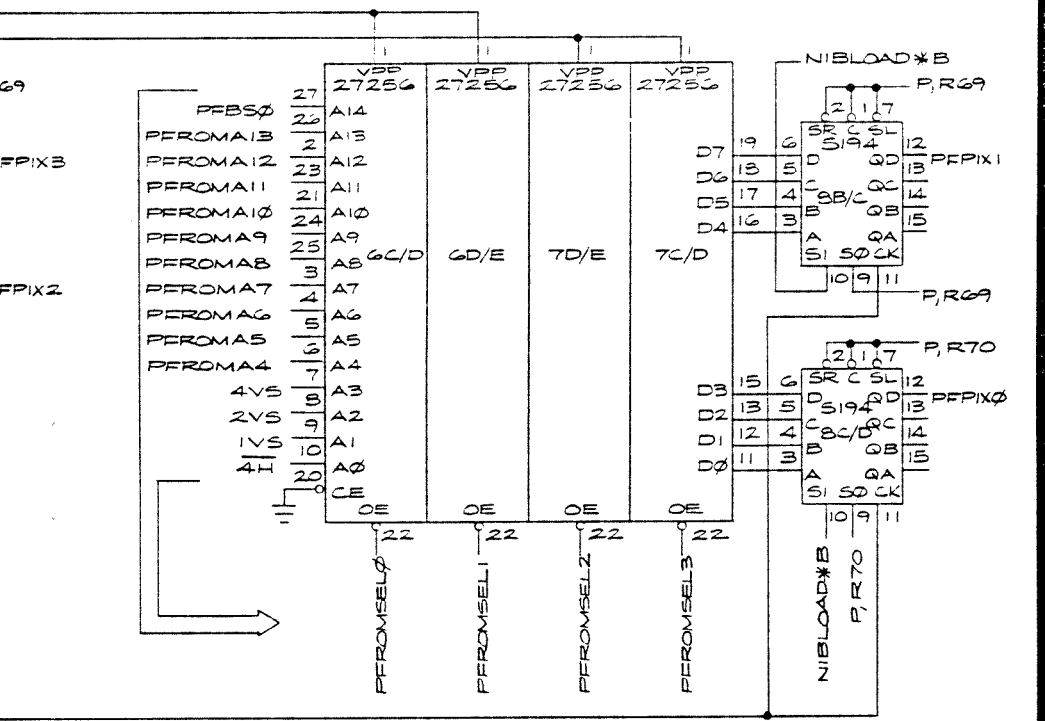
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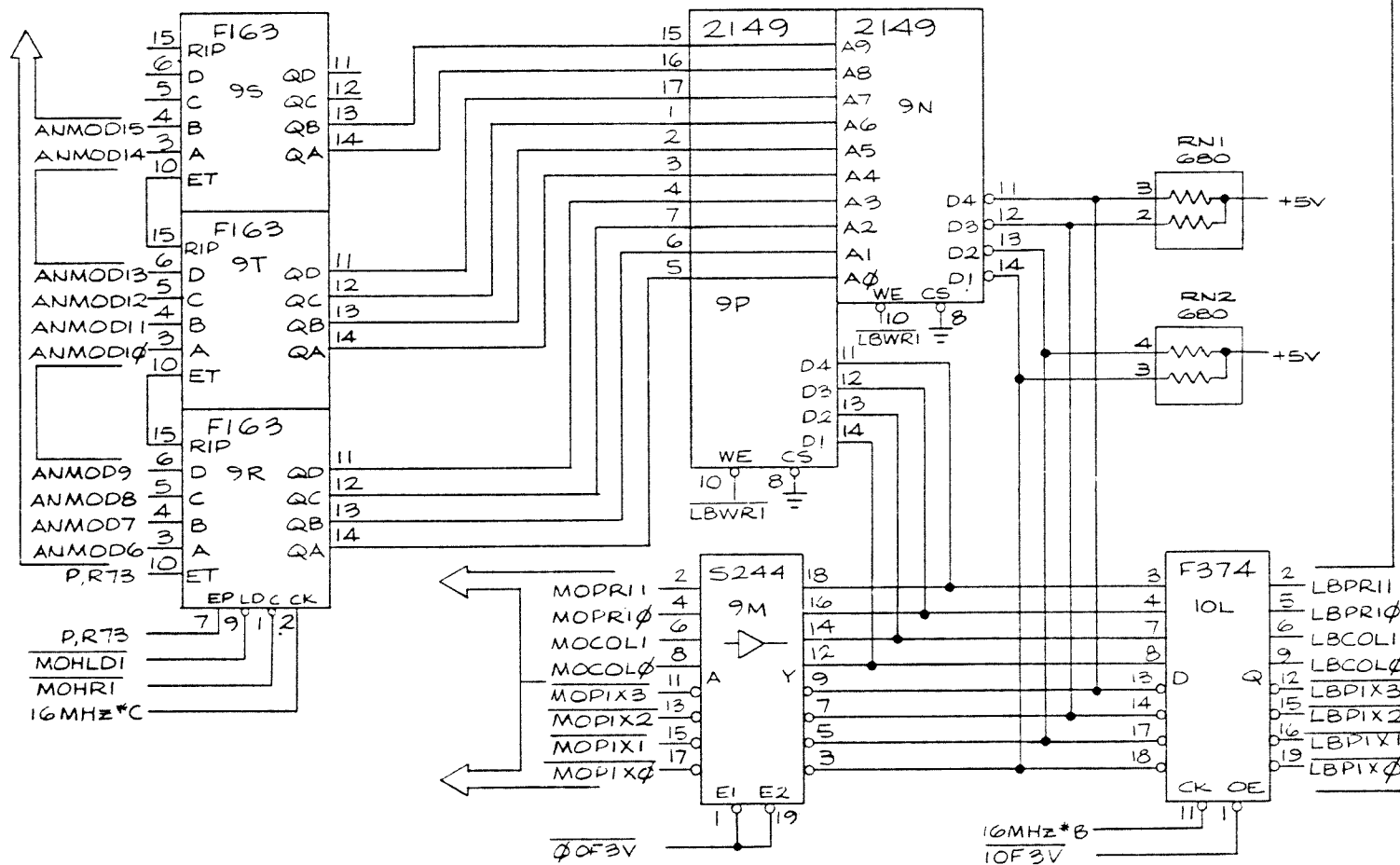
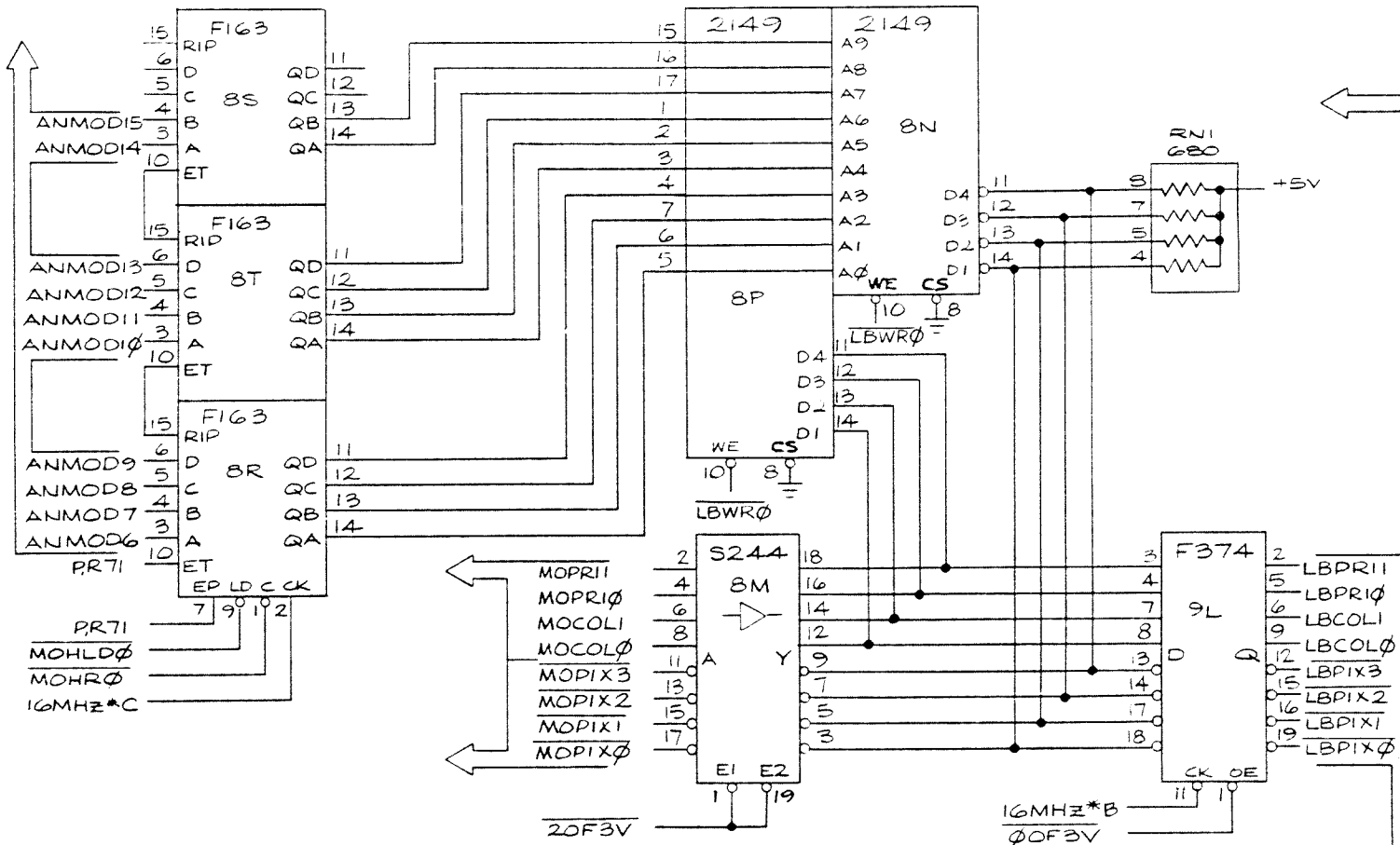
Playfield ROM

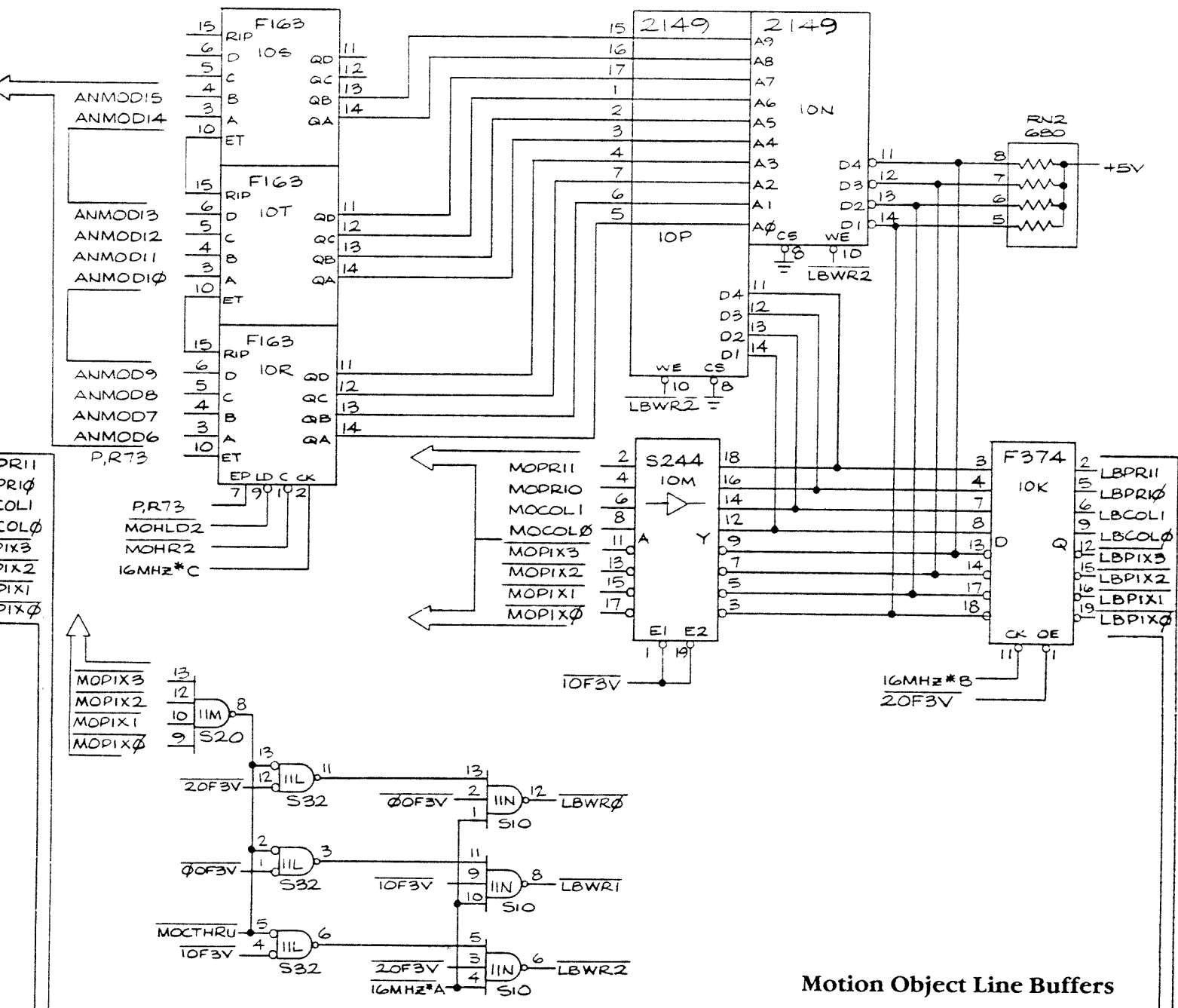
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Motion Object Line Buffers

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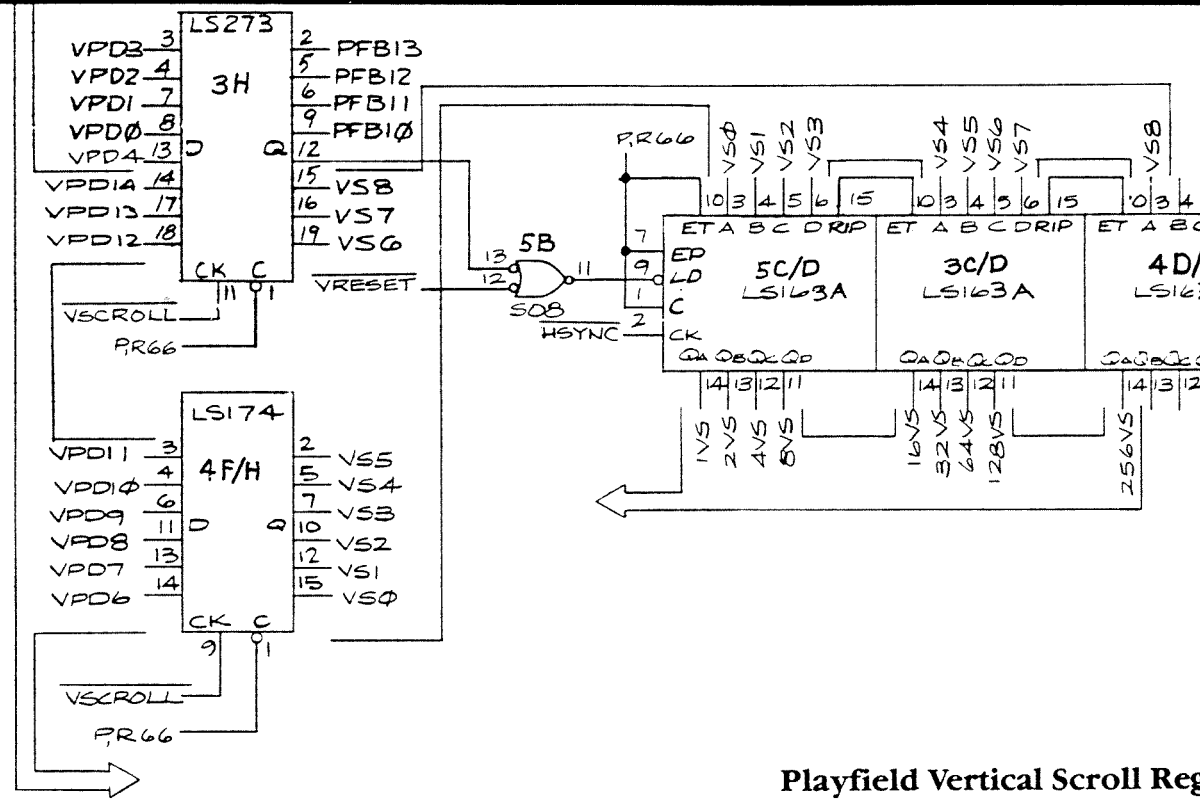
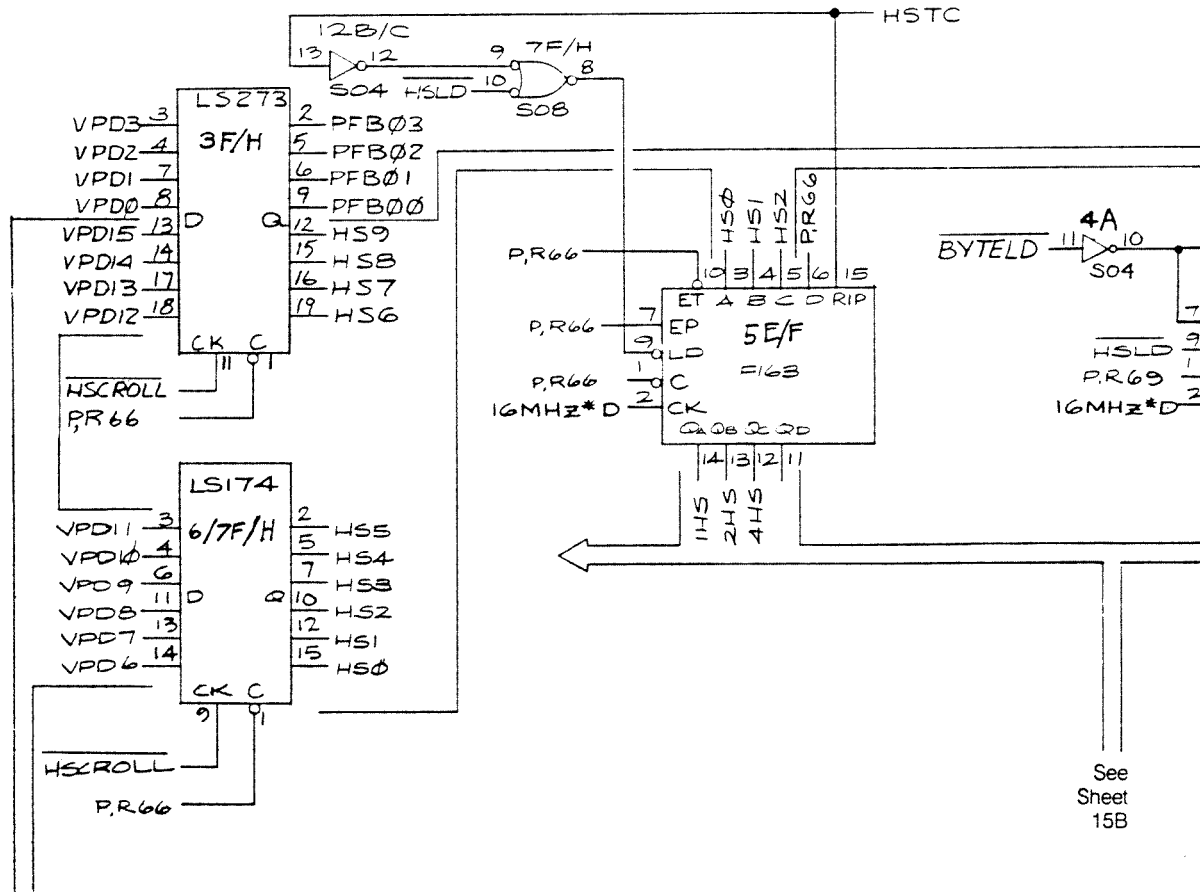
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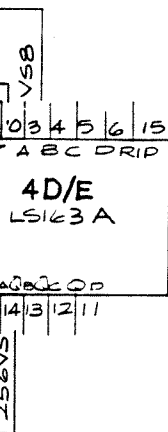
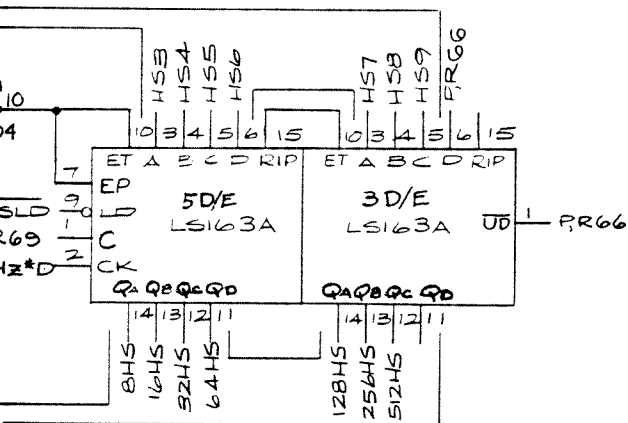
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Playfield Vertical Scroll Register

Playfield Horizontal Scroll Registers



all Registers

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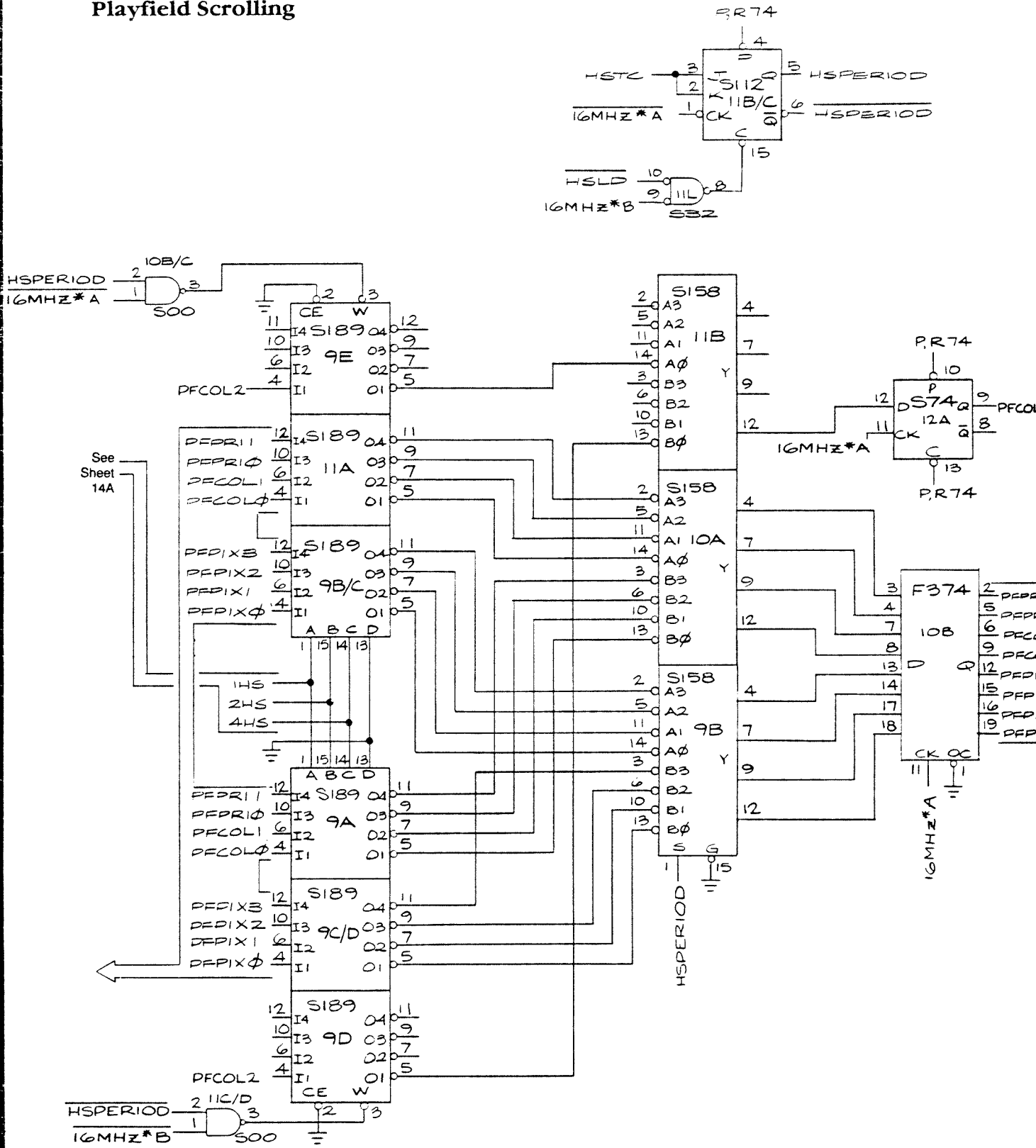


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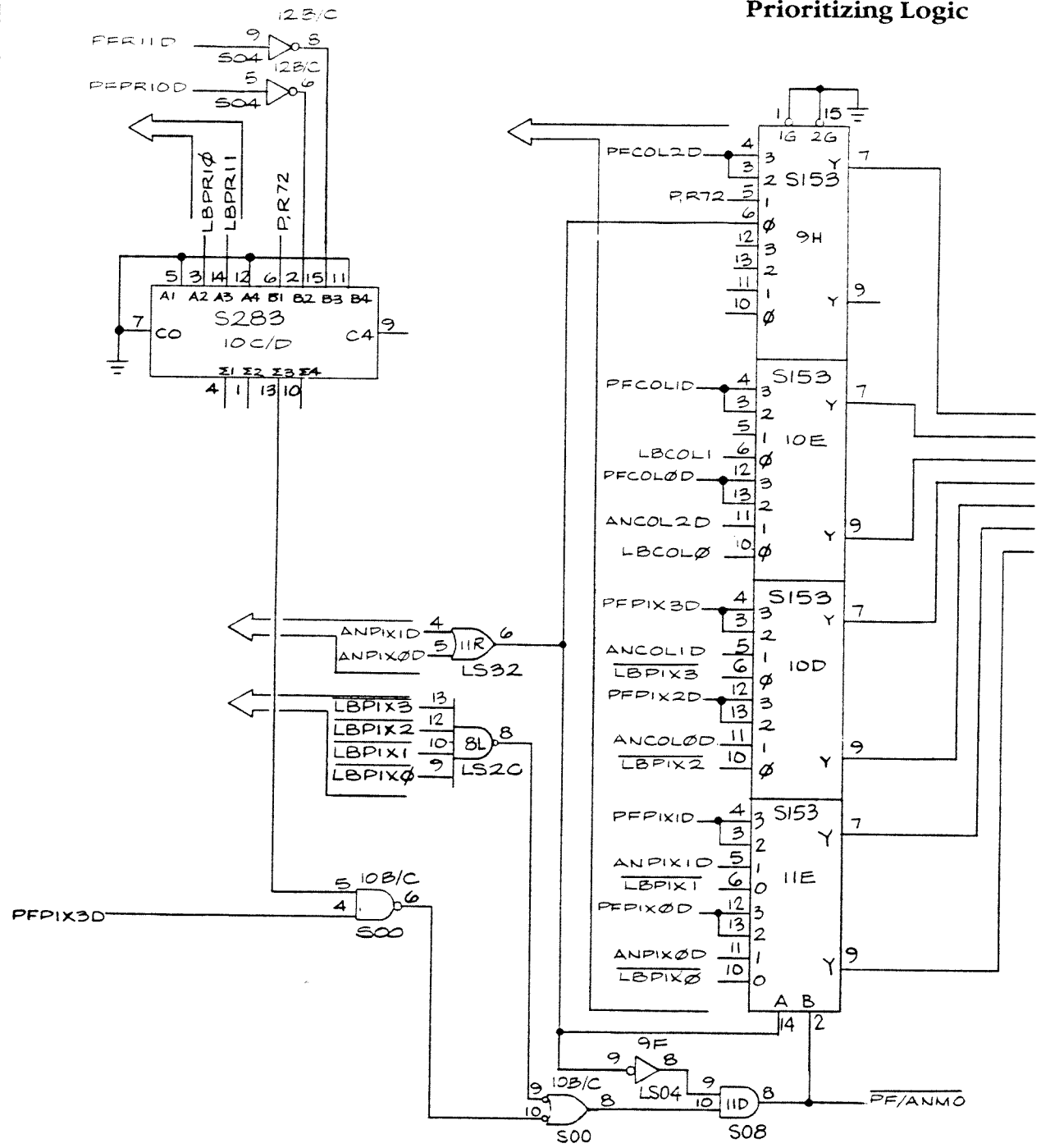
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Playfield Scrolling



Prioritizing Logic



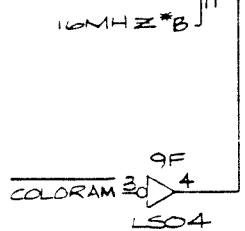
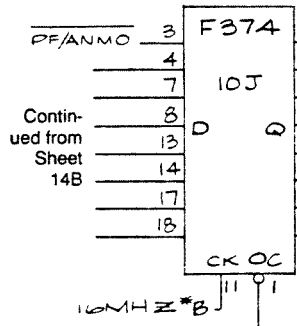
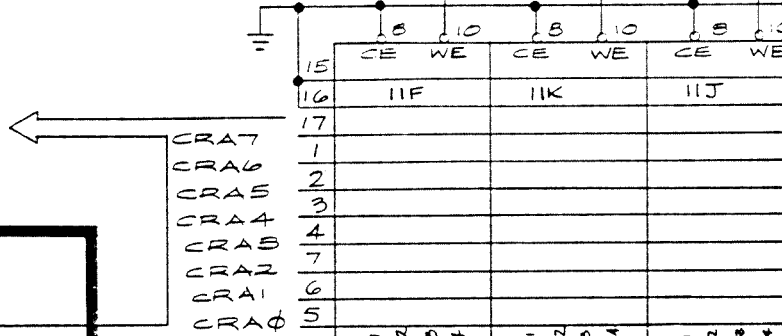
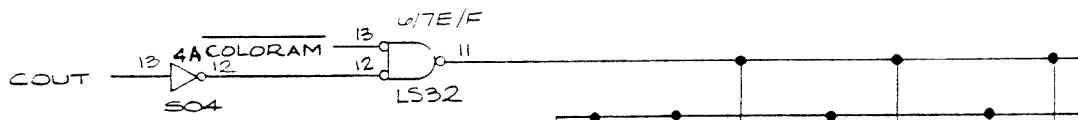
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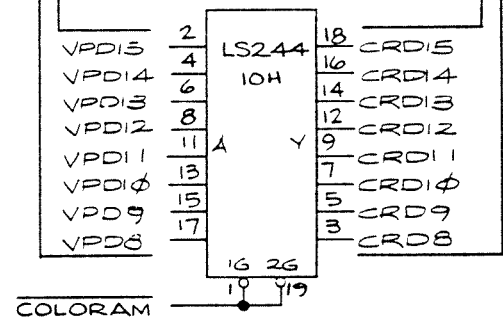
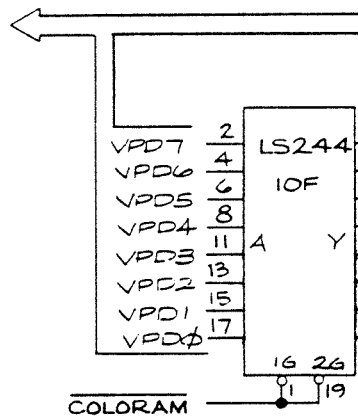
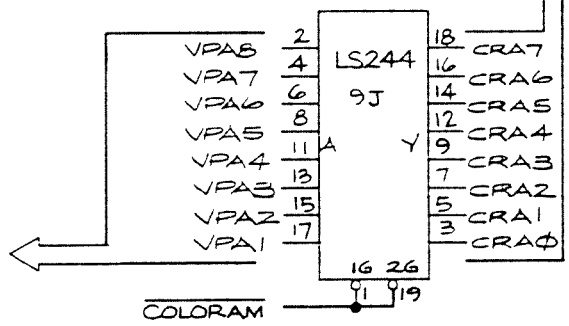


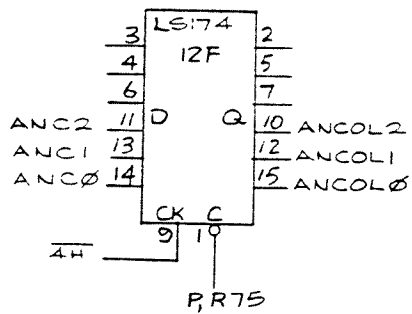
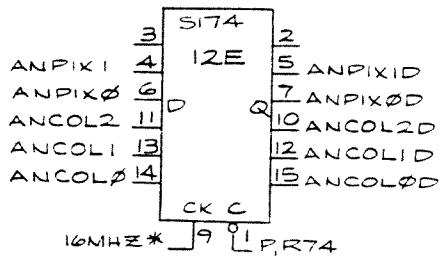
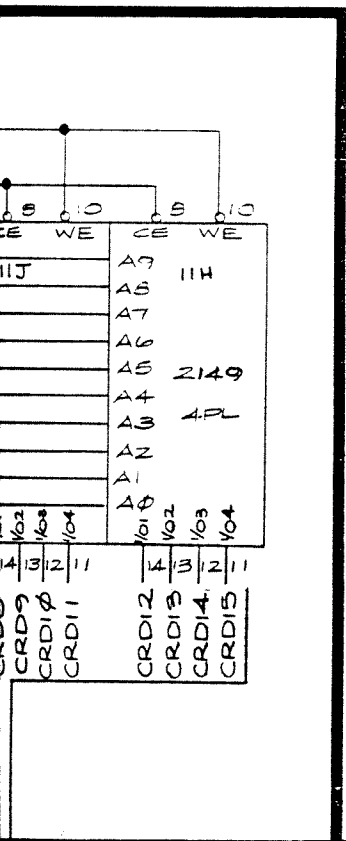
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Color RAM



Color RAM Addressing and Data Buffers





Alphanumeric Color Palettes Selects

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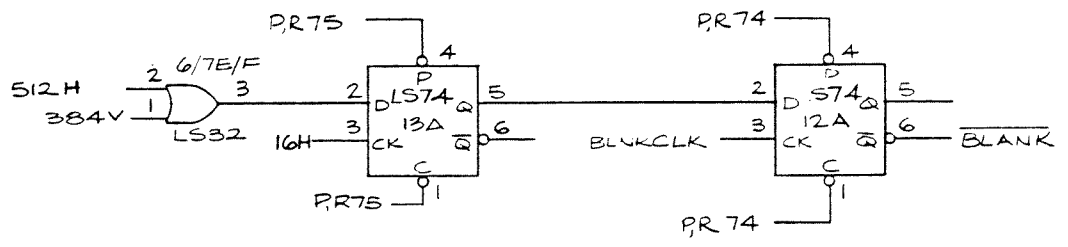
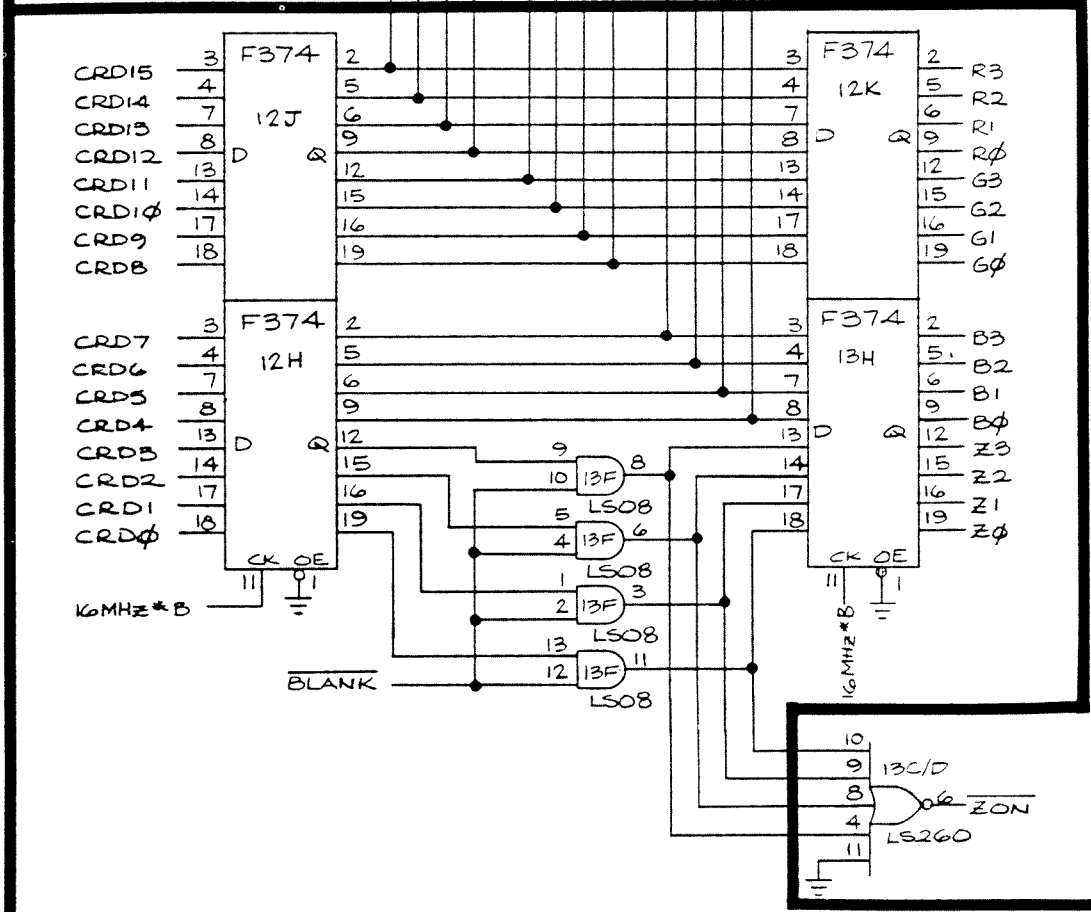
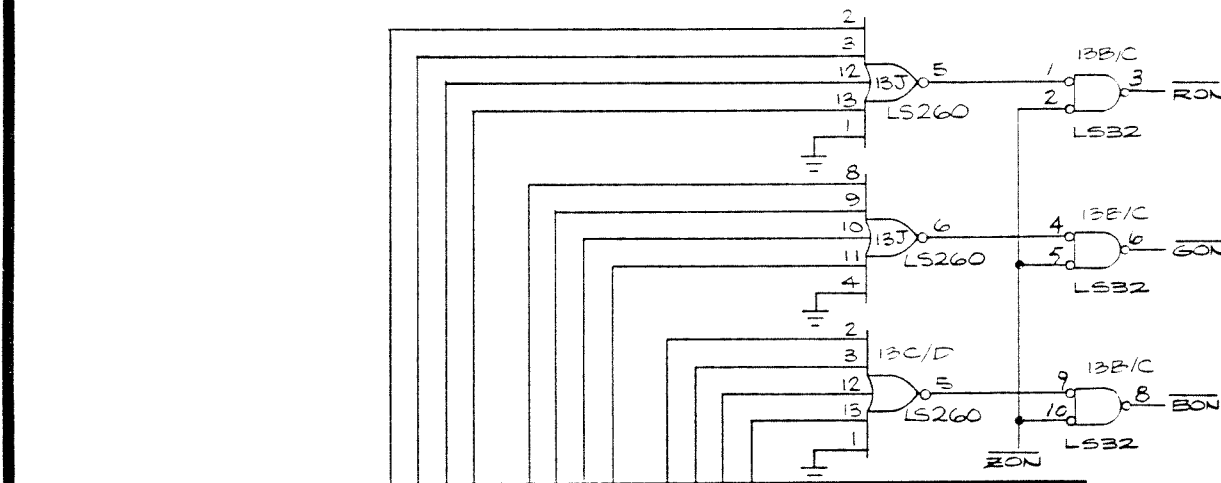


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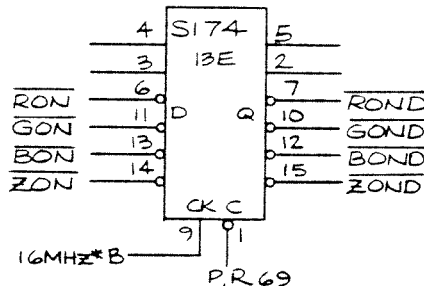
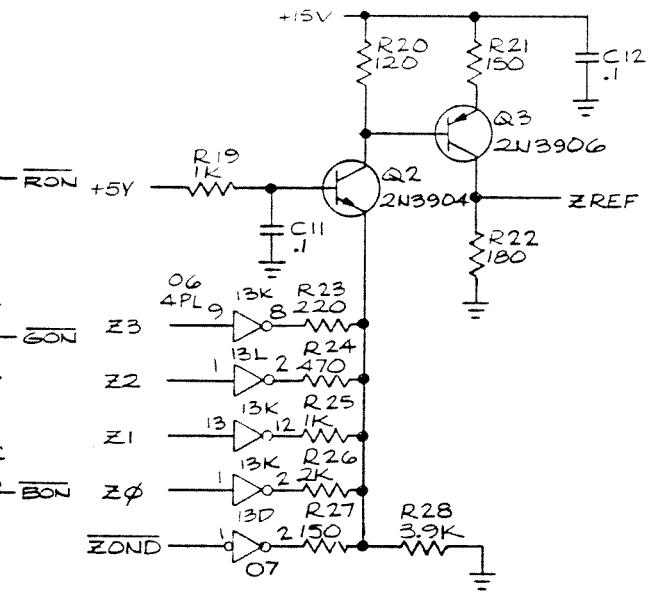
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Video Intensity Control and Driver Enables



Data Latches and Blanking



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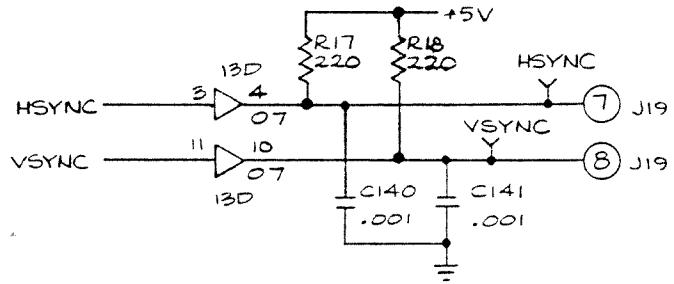
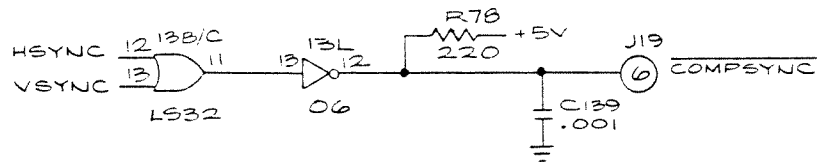
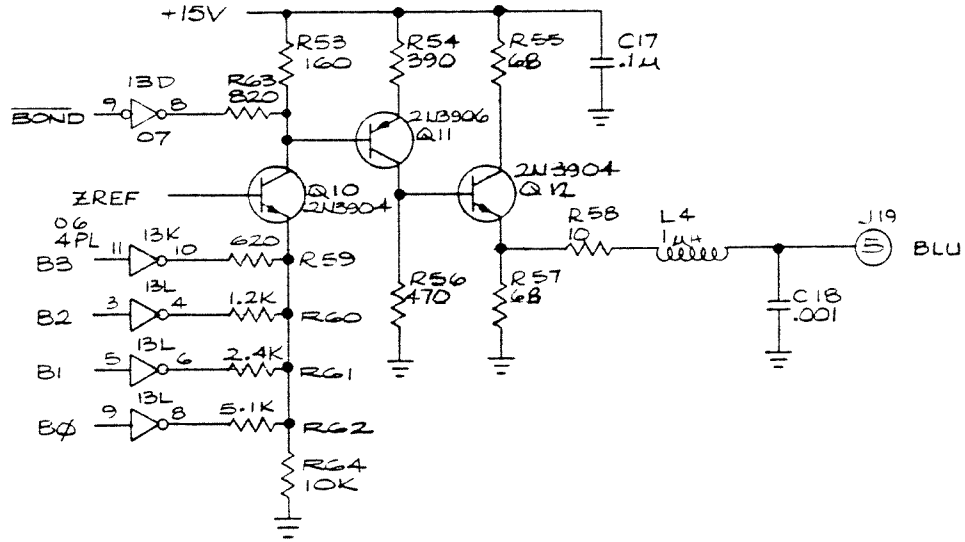
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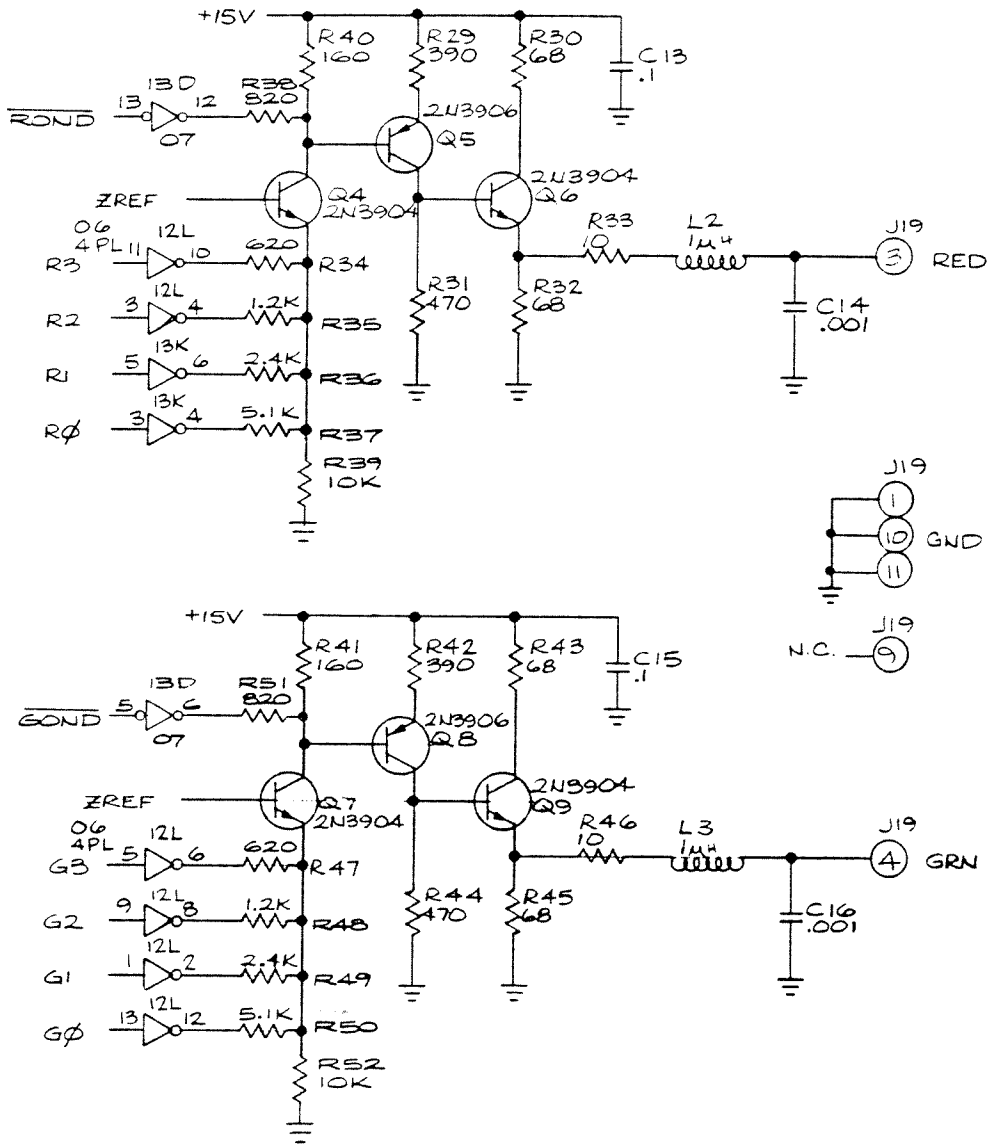
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Schematic Diagram**

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Output Drivers



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