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**Schematic Package Supplement to LIBERATOR**

**Operation, Maintenance, and Service Manual**

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SP-200 Sheet 1A
1st Printing
Coin-Door Wiring Diagram

Utility Panel Wiring Diagram

Coupler PCB Schematic

Fluorescent Light Wiring Diagram

Liberator™ Game Wiring Interfaces
## MEMORY MAP

<table>
<thead>
<tr>
<th>HEXA-DECIMAL ADDRESS</th>
<th>ADDRESS BUS</th>
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### Schematic Reference Designators and Symbols

Logic symbols depict the logic function performed by that particular device and may differ from the manufacturer’s data.

#### REFERENCE DESIGNATORS:
- **C**: Capacitor
- **D**: Diode, signal or rectifier
- **F**: Fuse
- **J**: Connector
- **L**: Inductor, fixed or variable
- **P**: Connector
- **Q**: Transistor or silicon-controlled rectifier
- **R**: Resistor, fixed or variable
- **S**: Switch
- **T**: Transformer
- **TP**: Twisted wire pair
- **VR**: Voltage regulator
- **Y**: Crystal

#### WIRE COLORS:
- **R**: Red
- **GN**: Green
- **Y**: Yellow
- **W**: White
- **BU**: Blue
- **BN**: Brown
- **OR**: Orange
- **V**: Violet
- **GY**: Gray

Electrical components shown on the schematic diagrams are in the following units unless otherwise noted:

- **Capacitors**: microfarads (µF)
- **Resistors**: ohms (Ω)
- **Inductors**: microhenrys (µH)

#### SYMBOLS:

- **Ground**: ⬤
- **PCB edge connector pad**: □
- **Test Point**: ○
- **PCB test connector pad**: ○

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To avoid faulty readings while testing signatures, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the entire test.

Liberator™ PCB Schematic Diagram
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SP-209 Sheet 7B
1st Printing
**Description of Liberator PCB Signal Names**

**A0-A15**
Address bits on Microprocessor Address Bus lines A0-A15 are software-generated by Microprocessor C2. When BITMD is low, A0-A15 are applied through buffers B1 and E1 to produce the bits on line A0B-A15.

**A0B-A13, A1B**
Address bits on Buffered Microprocessor Address Bus lines A0B-A10 are software-generated either by Microprocessor C2 or by BITMD and F1. When BITMD is low, A0B-A13 are generated via buffers B1 and E1. When BITMD is high and BITMD is low, Bit Map Address buffers H1 and F1 are generated to drive the lines on A0B-A13.

In the Address Decoders circuit, bits on lines A0B12 and A1B13 are the input signals for decoders T2, T3, and E4, and bits on lines A8B-A18 are input signals for decoder S2. Lines A0B-A11 carry the addresses for the Program Memory.

A1B1 is inverted by gate F4 to produce A1B11, A1B11 is a control bit for the clock on the Microprocessor C2. The bits on B1 and B2 are the address bits on the Address Output circuit. The bits on B1 and B2 are buffered at the base of Q5 and Q4 to drive the output address bus.

**BITMD**
The Bit Mode Enable signal is software-generated at pin 8 of Bit Map Address Decoder E4 during address 0002. BITMD is the output control signal for Bit Map Address Decoders H1 and F1. When BITMD goes low, the decoded address bits are driven through BITMD and are used in the Color Memory circuit. When BITMD goes high, the Color Memory address bits are driven from A0B-A13.

**BITMD**
The Bit Mode Disable signal is software-generated at pin 8 of Inverter F4. In the Bit Map Address Decoders circuit during address 0002, BITMD is the diode signal for buffers B1 and E1 of the Microprocessor circuit. When BITMD goes high, the buffers are tri-stated and the bit map address are put on the address bus.

**BNU**
The Blue signal is a game PCB output signal developed from the bits on B1 and B2. BU1 is generated at the emitter of Q4 in the Color or Output Circuit. The bits on B1 and B2 are summed at the base of Q5 and buffered by Q5 and Q4 to drive BLU.

**BMASEL**
The Bit Map Address Select signal is hardware-generated at pin 5 of latch E8 in the Refresh circuit. In the Bit Map Address circuit, BMASEL is the A select signal for Bit Map Address Multiplexers H9, H8, K9, and L8.

**B9**
The active high Level Phase 2 Clock signal is hardware-generated from the internal clock of Microprocessor C2 and filtered by Q2. B9 is gated with R10/69 and R10/70 to produce WHITE. B9 is also used as the clock for custom audio chips B3C and C3D in the Audio Output circuit.

**B/W**
The Black and White Video signal is a game PCB output signal that is generated at the emitter of Q11 in the Color Circuit output from COMPSTR, BLU, GRR, and RED. This signal can be used by a black and white video display when a color display is not available.

**C3**
The active low-level Column Address Select signal is hardware-generated at pin 9 of latch Q8 in the Refresh circuit. C3 is used to refresh the column address of the dynamic Bit Map Memory.

**CG3-C93**
The bits on Planet Color Code lines CG3-C93 are software-generated by Planet Picture ROMs P8 and M8.

**CLRDLWE**
The Clear/Load/Write Enable signal is hardware-generated at pin 9 of latch Q8 in the Multiplex Clock circuit. CLRDLWE is a control signal for the Multiplex Clock circuit.

**CONCOMMAND**
The Coin Counter Left signal is a game PCB output signal generated at the collector of Q3 in the Coin Door and Utility Panel Output circuit. CONCOMMAND is applied to the game utility panel to activate the Right Coin Counter.

**COLORAM**
The active low-level Color RAM Enable signal is software-generated at pin 2 of Address Decoder S2 during addresses 0B0-AB3 through 5B2F and is used in the Color Memory circuit. When COC DRAM is high, the Color Memory address bits are driven from A00-AB3.

**CORDERAM**
The Color Memory address bits are driven from B1-B11. When CORDERAM is high and the A select signal is high, the Color Memory address bits are driven from PLAY200-PLAY3. When both CORDERAM and CORDERAM go low, the Color Memories are enabled to write data.

**COMPSTR**
The active low-level Composite Syncronization signal is hardware-generated at pin 3 of gate M3 in the Vertical Sync Circuit by exclusive-ORing HSTC and VSYN. COMPSTR is applied directly to the video display circuitry for further processing.

**CTRLD**
The active low-level Control Load signal is generated at pin 9 of latches T11 in the Coin Counter and LED Output circuit. When CTRLD goes low, counters S11 and T11 are loaded from the Coins in Door and Control Panel Input switch.

**DO-D7**
Microprocessor Data Bus lines DO-D7 form a bidirectional data bus between the Microprocessor, the Program Memory, and the Audio Output circuits.

**D8-D87**
Buffered Microprocessor Data Bus lines D8-D87 form a buffered bidirectional data bus between microprocessor data bus buffers E2 and Bit Map Decoders H1 and F1. Bit Map Data Multiplexers H1 and P1, Bit Map Data Buffers T5, S9, and N9, Bit Map Memory T0, T1, T0, T0, and T0, LongDistance latch R1, Color Memories P11, C11, E11, and B11, EARCOM latches R2 and K2, EARCOM buffer H2, Coin Door and LED Output decoder T11, and Coin Door and Control Panel input multiplexers R1 and M1.

**DIRS**
The active high-level Display Initialize signal is generated at pin 8 of gate Q4 in the Planet Laram Memory Generator circuit. When high, DIRS clears counter M7 (and gate F9) clears latch ES. In the Lame Buffer Address Controller circuit, DIRS clears flip-flop K4 and counter H7.

**DISD**
Disable Data is an active low-level signal generated by test equipment connected to the DISD test point.

**DRAM1**
The Bit Map Data Bus lines DRAM1 are software-generated by the Bit Map Shift Registers. When BITMD, RAM, and RAVW are all low, the bits on DRAM-DRAM1 are passed through Bit Map Data Buffer T9 to the microprocessor data bus. When BITMD, RAM, and RAVW are all high, the bits on DRAM-DRAM1 are multiplexed by S9 and N9 of the Bit Map Data Buffer circuit and passed to lines B8-D84 of the microprocessor data bus.

When the Bit Map Shift Registers circuit, if LORAD is high, the bits on DRAM-DRAM1 are used by shift register R9 to produce BIT10; the bits on DRAM-DRAM1 are used by shift register R9 to produce BIT11; and the bits on DRAM-DRAM1 are used by shift register R9 to produce BIT12.

**EARCOM**
The Electrically Alterable Read-Only Memory Control signal is software-generated at pin 4 of Address Decoder S2 at address 690D. EARCOM is the clock signal for latch R2 in the EARCOM circuit. When high, EARCOM allows R2 to see data bits on lines D0B-D83 to the control lines of EAROM M2.

**EARD**
The Electrically Alterable Read-Only Memory Read Enable signal is software-generated at pin 12 of Address Decoder E4 at address 4000. EARD is the select signal for buffer H2 of the EARCOM circuit. When low, EARD allows the eight data bits from EAROM M2 to be passed through buffer H2 to the microprocessor data bus.

**EAHR**
The Electrically Alterable Read-Only Memory Write Enable is software-generated at pin 9 of Address Decoder S2 at address 690B through 693F. EAHWR is the clock signal for latches P7 and P2 in the EARCOM circuit. When low, EAHWR allows address bits on lines A0B-A05 and data bits on lines D8B-D87 to pass to the address and data input pins of EAROM M2.

**FSG**
The active high-level First Segment signal is the carry output of adder R17 in the LongDistance Slicing circuit. When FSG is high and LARD is high, the COE pin of address P7 is high. In addition, FSG is gated with PLS and HGR by gates R6, R2, and P3 in the Planet ROM Address Generator circuit to produce the clock signal for latch N7.

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GRN
The Green signal is a game PCB output signal derived from the bits on G0-G2. GRN is generated at the emitter of Q3 in the Color Output circuit. The bits on G0-G2 are summed at the base of Q9 and buffered by Q9 and Q10 to produce GRN.

HBLANK
The active high-level Horizontal Blanking signal is generated at pin 11 of counter P3 in the Horizontal Sync Chain. HBLANK is applied through inverter L3 to produce HBLANK. If HBLANK is high when latch T4 is clocked, HBLANK is set high and HBLANK is set low. When HBLANK goes low, HSTRIC from latch T4 is preset to the high state.

HBLANK
The active low-level Horizontal Blanking signal is hardwired-generated at pin 6 of inverter L3 in the Horizontal Sync Chain by inverting HBLANK. When low, HBLANK prepares HBLANK at latch T4 to the low state and HSTRIC at the high state. When the Horizontal Start/Stop Control circuit, when HBLANK goes low, it produces P0R from latch T3 to the high state and HSTRIC to the low state.

HBLANK
The active high-level Delayed Horizontal Blanking signal is hardwired-generated at pin 19 of latch T4 in the Horizontal Sync Chain. HBLANK is generated when HBLANK has been delayed by the gated result of bit 31 of 'H32'. HBLANK is the clock signal for latch M4 in the Vertical Sync Chain.

HBLANK
The active low-level Delayed Horizontal Blanking signal is hardwired-generated at pin 8 of latch T4 in the Horizontal Sync Chain. HBLANK is generated when HBLANK has been delayed by the gated result of bit 30 of 'H32'. HBLANK is the clock signal for latch M4 in the Vertical Sync Chain.

HBLANK
The active low-level Delayed Horizontal Blanking signal is hardwired-generated at pin 8 of latch T4 in the Horizontal Sync Chain. HBLANK is generated when HBLANK has been delayed by the gated result of bit 31 of 'H32'. HBLANK is the clock signal for latch M4 in the Vertical Sync Chain.

HSTRIC
The Horizontal Synchronization signal is hardwired-generated at pin 6 of latch T4 in the Horizontal Sync Chain. HSTRIC is generated at latch 3 when latch T4 is clocked by HSTRIC. HSTRIC is the clock signal for latch N8 and latch M5 in the Vertical Sync Chain. HSTRIC is also applied directly to the video display circuitry for further processing.

HBLANK
The active high-level Horizontal Blanking signal is hardwired-generated at pin 19 of latch T4 in the Horizontal Sync Chain. HBLANK is generated when HBLANK has been delayed by the gated result of bit 30 of 'H32'. HBLANK is the clock signal for latch M4 in the Vertical Sync Chain.

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The active low-level Horizontal Blanking signal is hardwired-generated at pin 19 of latch T4 in the Horizontal Sync Chain. HBLANK is generated when HBLANK has been delayed by the gated result of bit 30 of 'H32'. HBLANK is the clock signal for latch M4 in the Vertical Sync Chain.

HSTRIC
The Horizontal Synchronization signal is hardwired-generated at pin 6 of latch T4 in the Horizontal Sync Chain. HSTRIC is generated at latch 3 when latch T4 is clocked by HSTRIC. HSTRIC is the clock signal for latch N8 and latch M5 in the Vertical Sync Chain. HSTRIC is also applied directly to the video display circuitry for further processing.
PLA2
The Planet 2 Select signal is generated at pin 2 of inverter L3 in the Coin Counter and LED Output circuit by inverting PLA2. PLA2 is the chip select signal for Picture Plane ROMs P6 and R15.

PLANET
The Planet Enable signal is generated at pin 8 of chip D9 in the Planet Control circuit. PLANET changes state at a 5-MHz rate; either of the signals at pins 2 or 3 of D9 is high. When high, PLANET is used by Inset H5 to produce PLANET1 and PLANET2. When low, PLANET clears flip-flop K4 in the Display Counter and Comparator circuit.

PLANET1
The active high-level Disabled Planet Enable signal is generated at pin 9 of latch H5 in the Planet Control circuit. When PLANETD1 is high and counter D6 of the Display Counter and Comparator circuit has reached its minimum count, gate P4 produces the enable signal for Counter H6. At this time, counter H6 was previously loaded by HBANK going low, counter H6 beginning counting down.

PLANETD1
The Complementary Disabled Planet Enable signal is generated at pin 8 of latch H5 in the Planet Control circuit. When PLANETD2 is high and counter D6 of the Display Counter and Comparator circuit has reached its minimum count, gate P4 produces the enable signal for Counter H6. At this time, counter H6 was previously loaded by HBANK going low, counter H6 beginning counting down.

PLAYAVIDO
The Planet Video signals are software-generated by Line Buffers J7 and K7, latched by P6, and applied through multiplexers S5 and S5 to produce the Color Memory address bits.

PLS
The active high-level Planet Segment signal is hardware-generated at pin 8 of latch C8 in the Multiplex Clock circuit. In the Planet ROM Address Generator circuit, PLS is gated with FSG and HORB by pins R4, R3, and P3 to produce the clock signal for latch N7. In the Multiplexer circuit, PLS is the clock signal for latches F6 and D10.

RAM
The active low-level Random-Access Memory enable is software-generated at pin 4 of Address Decoder D2. RAM is gated with A2-A15 by gates G1 and C1 of the Bit Map Address Decoders to generate the enable signal for E4 in the Write Protection circuit. RAM is gated with WRITE to produce the clear signal for latch D5. In the RAM Data Buffer circuit, RAM is gated with BITMD and RWB by gate G3 to produce the enable signal for buffer T9.

RAS
The active low-level Row Address Select signal is hardware-generated at pin 8 of latch E8 in the Refresh circuit. RAS is used to refresh the row address of the dynamic Bit Map Memories.

RED
The RED signal is a game PCB output signal developed from the bits on R8–RJ. RED is generated at the emitter of Q6 in the Color Output circuit. The RED signal is summed at the base of QT and buffered by Q6 to Q8 to produce RED.

RESET1
Reset is an active low-level signal generated at pin 12 of counter J11 from either the Watchdog circuit or the Power-On Reset circuit. The Power-On Reset circuit sets RESET to an active low level either when the RESET test point is shorted to ground or during the time that the power-supply voltages are reaching their stabilized, regulated levels. This enables the Microprocessor Address Bus (A0–A15) is stabilized before Microprocessor C2 begins operation.

The Watchdog circuit sets RESET to an active low level if the microprocessor fails to output address counter before J11 has reached its maximum count.

RESET2
RESET2 is the clear signal for latches F2 in the IAPROM circuit and T11 in the Coin Counter and LED Output circuit.

ROM
The active high-level Read-Only Memory Enable signal is software-generated at pin 8 of gate H4 in the Address Decoders circuit during addresses 8B00 through EFFF. In the Microprocessor circuit, ROM is gated with FSG by gates H4 and H5 to enable bidirectional data bus buffer E2 to pass data. In addition, ROM is ANDed with CREDIT by gate H4 in the Program Memory circuit to enable buffer F2 to pass data.

ROM0
The active low-level Read-Only Memory Chip Select 0 signal is software-generated at pin 12 of Address Decoder D3 during addresses 8900 through 8AFF. ROM0 is the chip-select signal for Program Memory K11. When low, ROM0 allows K11 to be addressed and pass data to buffer F2.

ROM1
The active low-level Read-Only Memory Chip Select 1 signal is software-generated at pin 11 of Address Decoder D3 during addresses 8800 through 87FF. ROM1 is the chip-select signal for Program Memory K4. When low, ROM1 allows K4 to be addressed and pass data to buffer F2.

ROM2
The active low-level Read-Only Memory Chip Select 2 signal is software-generated at pin 10 of Address Decoder D3 during addresses A000 through AFFF. ROM2 is the chip-select signal for Program Memory K11. When low, ROM2 allows K11 to be addressed and pass data to buffer F2.

ROM3
The active low-level Read-Only Memory Chip Select 3 signal is software-generated at pin 12 of Address Decoder D2 during addresses C000 through DFF. ROM3 is the chip-select signal for Program Memory K20. When low, ROM3 allows K20 to be addressed and pass data to buffer F2.

ROM4
The active low-level Read-Only Memory Chip Select 4 signal is software-generated at pin 12 of Address Decoder D2 during addresses E000 through FFFF. ROM4 is the chip-select signal for Program Memory K31. When low, ROM4 allows K31 to be addressed and pass data to buffer F2.

ROM5
The active low-level Read-Only Memory Chip Select 5 signal is software-generated at pin 11 of Address Decoder D2 during addresses D000 through E0FF. ROM5 is the chip-select signal for Program Memory R51. When low, ROM5 allows R51 to be addressed and pass data to buffer F2.

ROM6
The active low-level Read-Only Memory Chip Select 6 signal is software-generated at pin 8 of gate P3 in the Address Decoders circuit during addresses 6600 through EFFF. ROM6 is the chip-select signal for Program Memory T1. When low, ROM6 allows T1 to be addressed and pass data to buffer F2.

T/R/W
The Buffered Read/Write/Load Enable signal is generated at pin 10 of inverter F4 in the Microprocessor circuit. RWB is gated with B10 and T4 by gates H4 and H3 to produce T/R/W in the Bit Map Data Buffers circuit. RWB is gated with RAM, BITMD, and BITMD by gate F3 to produce the enable signals for buffer T9 and multiplexers S9 and S6.

T/R/WB
The Buffered Read/Write/Load Enable signal is generated by Microprocessor C2, buffered by E3, and applied to custom audio chips B13/C3 and C6 in the Audio Output circuit and buffer E2 of the Microprocessor circuit. T/R/WB determines the direction of data flow through these devices.

SGCD–SGC4
The Planet Segment Code bits on lines SGCD1–SGC4 are hardware-generated by counter M7 in the Planet ROM Address Generator circuit. The bit on line SGCD4 is hardware-generated at pin 5 of latch E5. The Planet Segment Code provides the address bits for the Planet Picture ROM.

STARTLG
The active high-level Starting Longitude Enable signal is software-generated at pin 5 of latch E5. The Planet Segment Code provides the address bits for the Planet Picture ROM.

VSEEG
The active low-level Valid Segment signal is generated at pin 9 of latch E8. The Valid Segment signal is enabled by LORAST and LSEING by gates N4 and J4 to clock flip-flop K4 and enable a count-up operation by counter H7.

VSYNC
The active high-level Vertical Synchronization signal is hardware-generated at pin 8 of latch M4 in the Vertical Sync Circuit. VSYNC is exclusive-Orred with RSYNC by gate G3 to produce COUNTER/S. VSYNC is directed directly to the video display circuit for further processing.

WSDS
Watchdog Disable is a test point on pin 1 of gate L4 in the Watchdog circuit. When WDSD is grounded, RESET is prevented from going into an active low level (except when the RESET test point is grounded).

VBLANK
The active high-level Vertical Blank signal is hardware-generated at pin 11 of latch M4 in the Vertical Sync Circuit. VBLANK is applied to multiplexer M11 in the Coin Door and Control Panel Input circuit. When RD0 is low and A9 is high, VBLANK is used by Microprocessor C2 on data bus line DB7.

VBLANK
The active low-level Vertical Blank signal is hardware-generated at pin 10 of latch M4 in the Vertical Sync Circuit. VBLANK is gated by HBANK, by gate L4 of the Horizontal Sync Circuit to produce VBLANK.

VCLK1, VCK2
The Trak-Ball™ Vertical Clock signals are PCB input signals to the Trak-Ball™ Input circuit. When VBLKWP is high, VCLK1 is the clock signal for latch L11 and counter N11 in the Coin Door and Control Panel Input circuit; when VBLKP is low, VCK2 is the clock signal for latch L11 and counter N11.

VDRL1, VDR2
The Trak-Ball™ Vertical Directions signals are PCB input signals to the Trak-Ball™ Input circuit. When VBLKWP is high, VDR1 enables counter N11 in the Coin Door and Control Panel Input circuit to count; when VBLKP is low, VDR2 enables counter N11.

VBLANK
The active low-level Video Blank signal is hardware-generated at pin 6 of gate L4 in the Horizontal Sync Circuit. VBLANK is the clear signal for Color Memory latches A11 and D11.

VPA
The active low-level Vertical Planar Enable signal is hardware-generated at pin 2 of latch M4 in the Vertical Sync Circuit. VPA is gated with IP2SG by gate L4 in the Planar Control circuit to produce the clear signal for latch D9.

VSYNC
The active high-level Vertical Synchronization signal is hardware-generated at pin 8 of latch M4 in the Vertical Sync Circuit. VSYNC is exclusive-Orred with RSYNC by gate M3 to produce COUNTER/S. VSYNC is directed directly to the video display circuit for further processing.

WyDS
Watchdog Disable is a test point on pin 1 of gate L4 in the Watchdog circuit. When WDSD is grounded, RESET is prevented from going into an active low level (except when the RESET test point is grounded).

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Liberator™ PCB Signal Name Descriptions

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Description of Liberator PCB Signal Names (continued)

WDDS
The active low-level Watchdog signal is software-generated at pin 5 of Codec Decoder S2. WDDS is gated with WDD0 by gate L4 in the Watchdog circuit to produce the load signal for counter J1 of the Power-On Reset circuit.

WP-WP
The active low-level Write Pulse 0-3 are software-generated from gate B5 in the Write Protection circuit. These pulses are the write enable signals for the Bit Map Memories.

WRITE
The active low-level Write Enable signal is hardware-generated at pin 11 of gate G4 in the Microprocessor circuit. WRITE is applied to gate H3 in the Bit Map Address Decoders circuit where it is used to develop YCODR and XCODR. In the Write Protection circuit, WRITE is gated with RAM by gate N4 to produce the clear signal for latch D3. In the Address Decoders circuit, WRITE is applied to gate H3 to produce the D input signal for decoder S2.

X0-X7
The Planet Scaling bits are generated by latches F8 and D10 in the Multiplexor circuit. These bits are developed by those from the Longitude and Latitude Scaling circuits in the Wide Segment Detector. The bits on X0-X7 and those on LEDP are summed to produce VSEGD from the carry bit of adder F7.

XCOOD
The active high-level Pixel X Coordinate signal is software-generated at pin 3 of gate C8 in the Bit Map Y and X Decoders circuit during address 0000. XCOOD is the clock signal for Bit Map Decoder F1. When XCOOD goes high, E1 internally latches the data bits from D80-D87. Then, when BITDATA goes low, these bits are output from F1 to lines PK44-RX1 and A80-A88.

XCOOR
The active high-level Pixel Y Coordinate signal is software-generated at pin 11 of gate G3 in the Bit Map Address Decoders circuit during address 0000. YCODR is the clock signal for Bit Map Decoder H1. When YCODR goes high, H1 internally latches the data bits from D80-D87. Then, when BITMOD goes low, these bits are output from H1 to lines A96-A102.

H1
Horizontal Timing Signal 1 is hardware-generated at pin 10 of latch D6 in the Horizontal Sync Channel. H1 is ANDed with SMB1Y by gate F8 of the Refresh circuit for use in developing RAM in the Multiplexor circuit. H1 is ANDed with SMB2Y by gate F8 to produce the clock signal for latch D6. H1 is the clock signal for latch N3 of the Valied Segment Identification circuit. H1 is exclusive-ORed with the output signal at pin 14 of latch D4 by gate M3.

H1H
Complementary Horizontal Timing Signal 1 is hardware-generated at pin 9 of latch D9 in the Horizontal Sync Channel. In the Multiplexor circuit, H1H is gated with B40 and SMB2W by gates H4 and J4 to produce WRITE. H1H is NANDed with J4 by gate M4 of the Load Raster Control Circuit to develop the input signal for latch K3.

2H
Horizontal Timing Signal 2 is hardware-generated at pin 15 of counter E9 in the Horizontal Sync Channel. 2H is applied through inverter A8 to produce 2H. 2H is the timing reference for Microprocessor G2. In the Bit Map Address Multiplexer Circuit, 2H in the B select input for multiplexers L8, L9, J11, and H9. 2H is gated with 1H by gate N4 to produce the clear signal for Load Raster Control Latch K3. In the Multiplexor Circuit, 2H is ANDed with H7 by gate F6 to produce the clock signal for latch K7 in the Planar Control Circuit. 2H is exclusive-ORed with the output signal at pin 15 of latch D4 by gate M3.

2H
Complementary Horizontal Timing Signal 2 is hardware-generated at pin 15 of inverter A8 in the Horizontal Sync Channel. 2H is applied through inverter A8 to produce 2H. 2H is the clock signal for latch D5 in the Planet RAM Address Generator. In the Valid Segment Detector, 2H is gated with P4 to produce the input signal for latch N2. 2H is the clock signal for multiplexor K5 in the Base RAM circuit.

4H
Horizontal Timing Signal 4 is hardware-generated at pin 13 of counter E9 in the Horizontal Sync Channel. 4H is applied through inverter A8 to produce 4H. 4H is multiplexed with 2H, A88, and A80 by Bit Map Address Multiplexer H9.

4H
Complementary Horizontal Timing Signal 4 is hardware-generated at pin 13 of inverter A8 in the Horizontal Sync Channel. 4H is applied to gate J3 in the Line Buffer Address Controller to produce PINTZ.

8H
Horizontal Timing Signal 8 is hardware-generated at pin 12 of counter E9 in the Horizontal Sync Channel. 8H is ANDed with SMB2H by gate F8 to produce the clock signal for latch T4 in the Horizontal Sync Channel. 8H is multiplexed with 4H, A88, and A91 by Bit Map Address Multiplexer H9.

8H
Horizontal Timing Signal 16 is hardware-generated at pin 11 of counter E9 in the Horizontal Sync Channel. 16H is the clock signal for latch T4 of the Horizontal Sync Channel. 16H is multiplexed with 8H, A88, and A80 by Bit Map Address Multiplexer J9.

16H
Horizontal Timing Signal 32 is hardware-generated at pin 10 of counter F9 in the Horizontal Sync Channel. 32H is used in latch T4 of the Horizontal Sync Channel to produce the clock signals for latch D8, D10, A81, A89, and A85 by Bit Map Address Multiplexer J9.

48H
Horizontal Timing Signal 64 is hardware-generated at pin 13 of counter F9 in the Horizontal Sync Channel. 64H is multiplexed with 32V, A81, and A89 by Bit Map Address Multiplexer K9. In the Planet Control circuit, 64H is the clock signal for latch K3.

5MHHz
The 5 MHz clock signal is hardware-generated at pin 5 of Clock latch C3. 5MH is the internal clock for counters E9 and F9 in the Horizontal Sync Channel. In the Refresh circuit, 5MH is ANDed with 1H by gate F8. 5MH is the clock signal for Load Raster Control Latch K3 and Planet Control latch H5.

5MHHz
The Complementary 5 MHz clock signal is hardware-generated at pin 5 of Clock latch C3. 5MH is the internal clock for latch C5 in the Write Protection circuit. 5MH is the clock signal for Bit Map Shift Register M9, P9, and P10. In the Multiplexor, 5MH is the input signal for latches D6 and E8. In the Planet Control circuit, 5MH is the clock signal for latch D8. 5MH is gated with VSEGD and LDRAST by gates N4 and P4 in the Line Buffer Address Controller. In the Base RAM circuit, 5MH is gated with VSEGRM to produce the write enable signal for Base RAM L5. In the Color Memory, 5MH is the clock signal for latches H5 and D8. It is also gated with COLORCM by gate P4 to produce the write enable signal for Color RAMS B11, C11, E11, and F11.

10MHHz
The 10 MHz clock signal is hardware-generated at pin 9 of Clock latch BB. The 10 MHZ signal is used to clock latches E5 and E6 in the Refresh circuit, D8 of the Clock Multiplexor Circuit, and D5 of the Write Protection circuit. 10MH is ANDed with 8H by gate F8 in the Horizontal Sync Channel to produce the clock signal for latch T4. In the Multiplexor Circuit, 10MH is used by latch C9 to produce the CURLOWE and PLSS signals. In the Display Signals and Comparator Circuit, 10MH is gated with LBANCM by gate 89 to produce LATCH.

10MHHz
The Complementary 10 MHz clock signal is hardware-generated at pin 8 of Clock latch BB. 10MH is the clock signal for latch C9 in the Refresh circuit, devices D9, E9, and F9 in the Horizontal Sync Channel; counters B6 and E6 in the Display Counter and Comparator, and in the Color Memory. In addition, 10MH is gated with 20MH by gate E9 of the Display Counter and Comparator to produce the clock signal for flip-flop K4.

20MHHz
The 20 MHz clock signal is hardware-generated by crystal clock Y1 in the Clock Circuit. 20MH is the clock signal for latches B8 in the Clock Circuit and Display Counter and Comparator. 20MH is gated with 10MH by gate B9 to produce the clock signal for flip-flop K4.

20MHHz
The Complementary 20 MHz clock signal is hardware-generated at pin 4 of inverter A8 in the Clock Circuit. 20MH is the clock signal for latches C8 and D8 of the Multiplexor.

1V
Vertical Timing Signal 1 is hardware-generated at pin 14 of counter H8 in the Vertical Sync Channel. 1V and 2V are multiplexed by gate K8 and latched by M4 to produce VBANKL and VBLANK. Also, 1V is used by latch L8 to produce Y1LV. 1V is multiplexed with 128V, A13B, and A8B by Bit Map Address Multiplexer L9.

2V
Vertical Timing Signal 2 is hardware-generated at pin 15 of counter H8 in the Vertical Sync Channel. 2V and 3V are multiplexed by gate K8 and latched by M4 to produce VBANKL and VBLANK. Also, 2V is used by latch L8 to produce Y2LV. 2V is multiplexed with 4H, A87, and A50 by Bit Map Address Multiplexer H9.

4V
Vertical Timing Signal 4 is hardware-generated at pin 12 of counter H8 in the Vertical Sync Channel. 4V and 5V are multiplexed by gate K8 and latched by M4 to produce Y5LYC. Also, 4V is used by latch L8 to produce 4VLY. 4V is multiplexed with 8H, A8B, and A81 by Bit Map Address Multiplexer H9.

8V
Vertical Timing Signal 8 is hardware-generated at pin 11 of counter H8 in the Vertical Sync Channel. 8V and 9V are multiplexed by gate K8 and latched by M4 to produce Y5VSX. Also, 8V is used by latch L8 to produce 8VLY. 8V is multiplexed with 16H, A8B, and A82 by Bit Map Address Multiplexer J9.

16V
Vertical Timing Signal 16 is hardware-generated at pin 14 of counter J8 in the Vertical Sync Channel. 16V and 18V are multiplexed by gate K8 and latched by M4 to produce Y5PP. Also, 16V is used by latch L8 to produce 16VLYC. 16V is multiplexed with 8H, A88, and A80 by Bit Map Address Multiplexer J9.

32V
Vertical Timing Signal 32 is hardware-generated at pin 13 of counter J8 in the Vertical Sync Channel. 32V and 36V are multiplexed by gate K8 and latched by M4 to produce Y5PP. Also, 32V is used by latch L8 to produce 32VLYC. 32V is multiplexed with 8H, A88, and A80 by Bit Map Address Multiplexer J9.

64V
Vertical Timing Signal 64 is hardware-generated at pin 12 of counter J8 in the Vertical Sync Channel. 64V and 68V are multiplexed by gate K8 and latched by M4 to produce Y5PP. 64V is applied through inverter A8 to produce 64LYC. 64V is multiplexed with 128H, A10B, and A85 by Bit Map Address Multiplexer K9.
Description of Liberator PCB Signal Names (continued)

64V
Complementary Vertical Timing Signal 64 is hardware-generated at pin 8 of inverter A8 in the Vertical Sync Chain. 64V is used by latch L8 in the Vertical Sync Chain.

128V
Vertical Timing Signal 128 is hardware-generated at pin 11 of counter A11 in the Vertical Sync Chain. 128V and 64V are multiplexed by K6 and latched by M4 to produce VPLA. 128V is the clock 1 signal for counter J11 of the Power-On Reset circuit. 128V is also multiplexed with J11, A18, and A66 by Bit Map Address Multiplexer U4. 128V is applied with A23 to Base RAM decoder L7 to generate address bit 4 for Base RAM L5.

1VDL
Delayed Vertical Timing Signal 1 is hardware-generated at pin 5 of latch L8 in the Vertical Sync Chain. 1VDL is derived from 1V after a delay by HBLANK.1VDL is address bit 5 for Planet Picture ROMs P8, M/N, T8, and R/S8, and it is address bit 0 for Latitude Scalers P8 and N8.

2VDL
Delayed Vertical Timing Signal 2 is hardware-generated at pin 15 of latch L8 in the Vertical Sync Chain. 2VDL is derived from 2V after a delay by HBLANK.2VDL is address bit 6 for Planet Picture ROMs P8, M/N, T8, and R/S8, and it is address bit 1 for Latitude Scalers P8 and N8.

4VDL
Delayed Vertical Timing Signal 4 is hardware-generated at pin 9 of latch L8 in the Vertical Sync Chain. 4VDL is derived from 4V after a delay by HBLANK.4VDL is address bit 7 for Planet Picture ROMs P8, M/N, T8, and R/S8, and it is address bit 2 for Latitude Scalers P8 and N8.

8VDL
Delayed Vertical Timing Signal 8 is hardware-generated at pin 6 of latch L8 in the Vertical Sync Chain. 8VDL is derived from 8V after a delay by HBLANK.8VDL is address bit 8 for Planet Picture ROMs P8, M/N, T8, and R/S8, and it is address bit 3 for Latitude Scalers P8 and N8.

16VDL
Delayed Vertical Timing Signal 16 is hardware-generated at pin 2 of latch L8 in the Vertical Sync Chain. 16VDL is derived from 16V after a delay by HBLANK.16VDL is address bit 9 for Planet Picture ROMs P8, M/N, T8, and R/S8, and it is address bit 4 for Latitude Scalers P8 and N8.

32VOL
Delayed Vertical Timing Signal 32 is hardware-generated at pin 19 of latch L8 in the Vertical Sync Chain. 32VOL is derived from 32V after a delay by HBLANK.32VOL is address bit 10 for Planet Picture ROMs P8, M/N, T8, and R/S8, and it is address bit 5 for Latitude Scalers P8 and N8.

64VOL
Delayed Vertical Timing Signal 64 is hardware-generated at pin 13 of latch L8 in the Vertical Sync Chain. 64VOL is derived from 64V after a delay by HBLANK.64VOL is address bit 11 for Planet Picture ROMs P8, M/N, T8, and R/S8, and it is address bit 6 for Latitude Scalers P8 and N8.

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Liberator™ PCB Signal Name Descriptions

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SP-209 Sheet 11B
15th Printing
Liberator™ Troubleshooting with the CAT Box

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Troubleshooting with the Read/Write Controller

A. CAT Box Preliminary Set-Up
1. Remove the electrical power from the game and the CAT Box.
2. Remove the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet.
4. Remove Microprocessor C2 from the game PCB.
5. Connect the harness from the game to the game PCB.
6. Connect together the 90 and 42 test points on the game PCB with the shortest possible jumper.
7. Connect the WIDE test point to ground.
8. Connect the CAT Box flex cable to the game PCB edge test connector.
9. Apply power to the game and to the CAT Box.
10. Set CAT Box switches as indicated:
    a. TESTER SELF-TEST-OFF
    b. TESTER MODE: R/W
    11. Press TESTER RESET.
12. Connect the DATA PROBE to the CAT Box. Connect the DATA PROBE ground clip to a game PCB ground test point.

NOTE
To avoid faulty readings while performing these troubleshooting tests, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

B. Checking the Address Lines
1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/W MODE: UNLATCHED
   c. R/W MODE: (OFF)
   d. R/W: READ
3. Key in the address pattern given in Table 1 (use AAAA to start) with the CAT Box keyboard.
4. Set R/W MODE to STATIC.
5. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 1 lights up. Repeat this step for each address line listed in Table 1.
6. Repeat parts 2-6 using address 5555 in part 3.

Table 1 Address Lines

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<thead>
<tr>
<th>LOGIC STATE FOR ADDRESS AAAA</th>
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<th>LOGIC STATE FOR ADDRESS 5555</th>
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</table>

C. Checking the Data Lines
1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: ADDR
   b. BYTES: 128
   c. R/W MODE: (OFF)
   d. R/W: WRITE
3. Key in address 0000 with the keyboard.
4. Press DATA SET. Key in data A4 with the keyboard.
5. Set R/W MODE to PULSE and back to (OFF).
6. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 2 lights up. Repeat this check for each IC-pin in Table 2.
7. Repeat parts 4 through 6 using data 55 in part 4.

Table 2 Data Lines

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<th>IC-PIN</th>
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</table>

D. Checking the RAM
1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: ADDR
   b. BYTES: 128
   c. R/W MODE: (OFF)
   d. R/W: WRITE
3. Enter address 0000 with the keyboard.

NOTE
Addresses 0000, 0001, and 0002 are special RAM locations for bit mode operation that can not be verified by this RAM test.

Continued on back of sheet

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Liberator™ PCB Troubleshooting

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1st Printing
4. Set the CAT Box switches as indicated:
   a. R/W/MODE to PULSE and back to (OFF)
   b. R/W/READ
   c. R/W/MODE to PULSE and back to (OFF)
5. If the CAT Box reads an address that doesn’t compare with that written, the COMPARE ERROR LED will light up. The ADDRESS-SIGNATURE display of the CAT Box will show the failing address location and the ERROR DATA DISPLAY switch is enabled. Using this switch, determine if the error is in the high-order or low-order RAM.
6. Repeat parts 2 d through 4 using addresses 0400, 0600, 0C00, 1000, 1400, 1800, 1C00, 2000, 2400, 2800, 2C00, 3000, 3400, 3800, and 3C00.
7. Repeat this test with DBUS SOURCE set to ADDR.

E. Checking the Custom Audio I/O Chips

NOTE

Liberator has two custom audio I/O chips. Each must be tested separately. There are several ways to test these chips:
- Perform the self-test.
- Substitue a known good part for a suspected defective part.
- Use the following procedure.

1. Perform the CAT Box preliminary setup.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/W: WRITE
   c. R/W/MODE: (OFF)
3. Enter the address from Table 3 with the keyboard.
4. Press DATA SET and enter the data from Table 3 with the keyboard.
5. Set R/W/MODE to PULSE and back to (OFF).
6. Repeat parts 3 through 5 for each address and data listed in Table 3. Check for the response indicated.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
<th>TEST RESULTS</th>
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<tbody>
<tr>
<td>7800</td>
<td>00</td>
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</tr>
<tr>
<td>7801</td>
<td>03</td>
<td></td>
</tr>
<tr>
<td>7802</td>
<td>55</td>
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<td>7803</td>
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<th>ADDRESS</th>
<th>DATA</th>
<th>TEST RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>7801</td>
<td>00</td>
<td>Custom Audio I/O Chip B3 channel 1 produces pure tone.</td>
</tr>
<tr>
<td>7802</td>
<td>00</td>
<td>Custom Audio I/O Chip B3 channel 1 off.</td>
</tr>
<tr>
<td>7803</td>
<td>55</td>
<td>Custom Audio I/O Chip B3 channel 2 produces pure tone.</td>
</tr>
<tr>
<td>7803</td>
<td>00</td>
<td>Custom Audio I/O Chip B3 channel 2 off.</td>
</tr>
<tr>
<td>7900</td>
<td>00</td>
<td></td>
</tr>
<tr>
<td>7901</td>
<td>03</td>
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<td>55</td>
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<th>ADDRESS</th>
<th>DATA</th>
<th>TEST RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>7901</td>
<td>00</td>
<td>Custom Audio I/O Chip C/D3 channel 1 produces pure tone.</td>
</tr>
<tr>
<td>7902</td>
<td>00</td>
<td>Custom Audio I/O Chip C/D3 channel 1 off.</td>
</tr>
<tr>
<td>7903</td>
<td>55</td>
<td>Custom Audio I/O Chip C/D3 channel 2 produces pure tone.</td>
</tr>
<tr>
<td>7903</td>
<td>00</td>
<td>Custom Audio I/O Chip C/D3 channel 2 off.</td>
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F. Checking the Player Switch, Option Switch, and Trak-Ball™ Inputs

1. Perform the CAT Box preliminary setup.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/W: WRITE
   c. R/W/MODE: (OFF)
3. Enter address 6C04 with the keyboard.
4. Press DATA SET and enter data 00 with the keyboard.
5. Set R/W/MODE to PULSE and back to (OFF). The CTRLD signal is now set to the low state.
6. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/W: READ
   c. R/W/MODE to (OFF)
7. For each address listed in Table 4, do the following:
   a. Set R/W/MODE to (OFF).
   b. Enter the address with the keyboard.
   c. Set R/W/MODE to STATIC.
   d. Activate the input switch indicated in Table 4 for the address and check the test result.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>INPUT SWITCH</th>
<th>TEST RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>5000</td>
<td>Slam, Right coin switch, Left coin switch, Self Test switch, Auxiliary coin switch</td>
<td>DATA display changes when any coin or self-test switch is activated.</td>
</tr>
<tr>
<td>5001</td>
<td>FIRE 1, SHIELD 1, FIRE 2, SHIELD 2, START 1, START 2</td>
<td>DATA display changes when any of these switches is activated. (Note that display changes also without activating a switch because of VBLANK).</td>
</tr>
</tbody>
</table>

G. Checking the LED and Coin Counter Outputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES: 1
   c. R/W: WRITE
   d. R/W/MODE: (OFF)

CAUTION

If you write ON data to activate a solenoid, deactivate the solenoid immediately by writing the OFF data. If you leave a solenoid activated for more than 10 seconds, you may have to replace the solenoid and/or its driver, due to overheating.

3. For each address listed in Table 6, do the following:
   a. To activate the output:
      - Press DATA SET.
      - Enter data 00 with the keyboard.
      - Set R/W/MODE to STATIC and back to (OFF).
   b. To deactivate the output:
      - Press DATA SET.
      - Enter data FF with the keyboard.
      - Set R/W/MODE to STATIC and back to (OFF).

Continued on next sheet
Troubleshooting with Signature Analysis

A. Checking the Address Lines and Address Decoders

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES:
   c. I/W WRITE
   d. I/W MODE: (OFF)
3. Enter address 0000 with the keyboard.
4. Press DATA SET and enter data 00 with the keyboard.
5. Set I/W MODE to IC and back to (OFF).
6. Enter address 0001 with the keyboard.
7. Press DATA SET and enter data 00 with the keyboard.
8. Set I/W MODE to STATIC and back to (OFF).
9. Connect the three BNC-to-EZ clip cables supplied with the CAT Box to the signature analysis CONTROL, START, STOP, and CLOCK jacks of the CAT Box.
10. Connect the three black EZ clips to a game PCB ground test point.
11. Ground pin 4 of IC H4 (the DSDAT signal) on the game PCB.
12. Set the CAT Box switches as indicated:
    a. TESTER MODE: SIG
    b. TESTER SELF-TEST: OFF
    c. PULSE MODE: LATCHED
    d. START: Negative-going edge trigger
    e. STOP: Negative-going edge trigger
    f. CLOCK: Negative-going edge trigger
13. Press TESTER RESET on the CAT Box.
14. Connect the CAT Box Signature Analysis probe tips as indicated:
    a. START: Pin 3 of IC T2
    b. STOP: Pin 3 of IC T2
    c. CLOCK: 42 test point
15. Verify the set-up connections by connecting the DATA PROBE to a game PCB ground test point. The CAT Box ADDRESS/SIGNATURE display should show 0000. Now connect the DATA PROBE to a +5V test point. The ADDRESS/SIGNATURE display should show 0001.
16. Probe the IC pin listed in Table 7 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC pin listed.

B. Checking the Planet-Generating Circuity

1. Perform steps 1 through 7 of the CAT Box preliminary set-up.
2. Connect the CAT Box Signature Analysis probe tips where indicated:
   a. START: Pin 11 of IC E9
   b. STOP: Pin 11 of IC E9
   c. CLOCK: Pin 8 of IC B8
3. Connect the ground clips of the CAT Box Signature Analysis and DATA probes to a game PCB ground test point.
4. Set the CAT Box switches as indicated:
   a. TESTER MODE: SIG
   b. TESTER SELF-TEST: OFF
   c. PULSE MODE: UNLATCHED
   d. START: Positive-going edge trigger
   e. STOP: Positive-going edge trigger
   f. CLOCK: Positive-going edge trigger
5. Turn on the game and the CAT Box.
6. Verify these set-up connections by connecting the CAT Box ADDRESS/SIGNATURE display for A76.
7. Test the signatures designated by (XXXX) printed in color on the schematic diagrams of the game PCB. To test for a signature, use the CAT Box DATA PROBE to probe the appropriate location on the game PCB. Then check the ADDRESS/SIGNATURE display for the appropriate signature.

NOTE
To avoid faulty readings while performing these troubleshooting tests, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

8. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated by (XXXX)\(\) on the schematics.
9. Connect the CAT Box Signature Analysis probe tips to:
   a. START: Pin 11 of IC F9
   b. STOP: Pin 11 of IC F9
10. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for 1308.
11. Set the CAT Box CLOCK switch for a positive-going edge trigger and test the signatures designated on the schematics by (XXXX)\(\).
12. Connect the CAT Box Signature Analysis probe tips to:
    a. START: Pin 11 of IC J8
    b. STOP: Pin 11 of IC J8
13. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for H57U.
14. Test the signatures designated on the schematics by (XXXX)\(\).

NOTE
To avoid faulty readings while performing these troubleshooting tests, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

15. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated on the schematics by (XXXX)\(\).
16. Remove the electrical power from the game and the CAT Box.
17. Connect the CAT Box Flex cable to the game PCB edge test connector and connect the game PCB FSon test point to ground.
18. Apply power to the game and the CAT Box.

---

Table 6 LED and Coin Counter Outputs

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
<th>OUTPUT DEVICE</th>
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<tr>
<td>6CO0</td>
<td>ON</td>
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<td>6CO1</td>
<td>ON</td>
<td>OFF</td>
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<tr>
<td>6CO4</td>
<td>LOW HIGH</td>
<td>CTRED</td>
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<td>6CO5</td>
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<td>OFF</td>
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<tr>
<td>6CO6</td>
<td>OFF</td>
<td>ON</td>
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<td>6CO7</td>
<td>OFF</td>
<td>PLANET</td>
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Table 7 Address Bus Signatures

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<td>E1-18</td>
<td>AB5</td>
<td>U6/6U</td>
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<td>E1-16</td>
<td>AB1</td>
<td>5550</td>
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<td>E1-14</td>
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<td>CCC</td>
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<td>E1-12</td>
<td>AB3</td>
<td>777F</td>
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<td>B1-3</td>
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Table 8 Decoder Signatures

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<td>E4-0</td>
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<td>XCOORD</td>
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<td>E5D</td>
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<td>IN0</td>
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<td>ROM0</td>
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<td>A711</td>
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<td>54FS</td>
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<td>P3-8</td>
<td>ROM6</td>
<td>P255</td>
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</tbody>
</table>

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1st Printing
19. Set the CAT Box switches as indicated:
   a. TESTER MODE: R/W
   b. BYTES: 1
   c. R/W: WRITE
   d. R/W MODE: (OFF)
20. Press TESTER RESET.
21. Enter address 6600 with the keyboard.
22. Press DATA SET and enter data 00 with the keyboard.
23. Set R/W MODE to PULSE and back to (OFF).
24. Enter address 6007 with the keyboard and repeat steps 22 and 23.
25. Set the CAT Box switches as indicated:
   a. TESTER MODE: SIG
   b. START: Negative-going edge trigger
   c. STOP: Negative-going edge trigger
   d. CLOCK: Positive-going edge trigger
26. Connect the CAT Box Signature Analysis probe tips to:
   a. START: Pin 12 of IC L8
   b. STOP: Pin 12 of IC L8
   c. CLOCK: Pin 10 of IC A8
27. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for 6600.
28. Test the signatures designated on the schematics by (XXXX)4.

**NOTE**
To avoid faulty readings while performing these troubleshooting tests, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

29. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated on the schematics by (XXXX)4.
30. Set TESTER MODE to R/W and enter address 6600 with the keyboard.
31. Press DATA SET and enter data 7F with the keyboard.
32. Set R/W MODE to PULSE and back to (OFF).
33. Set the CAT Box switches as indicated:
   a. TESTER MODE: SIG
   b. START: Positive-going edge trigger
   c. STOP: Negative-going edge trigger
   d. CLOCK: Positive-going edge trigger
34. Connect the CAT Box Signature Analysis probe tips to:
   a. START: Pin 2 of IC M4
   b. STOP: Pin 2 of IC M4
35. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for 6600.
36. Test the signatures designated on the schematics by (XXXX)6.

**NOTE**
To avoid faulty readings while performing these troubleshooting tests, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

37. Connect pin 8 of IC P4 and connect test point PSIG2 to a game PCB ground test point.
38. Set TESTER MODE to R/W and enter address 6600 with the keyboard.
39. Press DATA SET and enter data 6000 with the keyboard.
40. Set R/W MODE to PULSE and back to (OFF).
41. Repeat steps 38 through 40 for addresses 6001, 6002, 6003, 6004, 6005, 6006, 6007, 6008, 6009, 600A, 600B, 600C, 600D, 600E, 600F, and 6000.
42. Set TESTER MODE to SIG.
43. Connect the CAT Box CLOCK probe tip to pin 8 of IC G6.
44. Verify these set-up connections by checking the CAT Box ADDRESS/SIGNATURE display for 6600.
45. Test the signatures designated on the schematics by (XXXX)6.

**NOTE**
To avoid faulty readings while performing these troubleshooting tests, take care NOT to short-circuit two or more leads with the CAT Box DATA PROBE. Should this accidently occur, you must again perform the test from its start.

46. Set the CAT Box CLOCK switch for a negative-going edge trigger and test the signatures designated on the schematic by (XXXX)6.
47. Remove the ground connection from pin 8 of IC P4 and from test point PSIG2.
48. Connect the CAT Box CLOCK probe tip to pin 14 of IC G9 and set the CLOCK switch for a positive-going edge trigger.
49. Test the signatures designated on the schematics by (XXXX)6.

---

**Troubleshooting with Checksums**

**NOTE**
This procedure can only be done with those CAT Boxes equipped with a Checksum Switch.

**CAUTION**
While testing with checksums, adding 100 pf capacitors to A14 and A15 may be necessary.

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as indicated:
   a. BYTES: 256
   b. DBUS SOURCE: DATA
   c. R/W MODE: OFF
   d. CHECKSUM SWITCH: ON
3. Key in the address pattern given in Table 9 (use 6000 to start).
4. Set the R/W MODE switch to PULSE and then back to (OFF).
5. Check the CAT Box ADDRESS/SIGNATURE display for the appropriate checksum.
6. Repeat parts 3 through 5 for each address listed in Table 9.

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**Troubleshooting the Watchdog Circuit**

The Watchdog circuit will send continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuit. If the self-test fails to run, it is a good practice to check the reset line.

RESET is a microprocessor input pin (pin 40). In a properly operating game, reset should occur during power-up or when the RESET test point is grounded. A pulsing RESET line indicates that something is causing the microprocessor to lose its place within the program. Typical causes are:

1. Open or shorted address or data bus lines.
2. Bad microprocessor chip.
3. Bad bus buffers.
4. Bad ROM.
5. Bad RAM.
6. Any bad input or output that causes an address or data line to be held in a constant high or low state.

A pulsing RESET signal indicates a problem exists somewhere within the microprocessor circuitry rather than within the analog vector-generator. To aid in troubleshooting, the MOOS test point can be connected to a ground test point to prevent resets. This will sometimes allow the Self-Test to be used to diagnose the failure during a RESET condition.

---

**Table 9 ROM Checksums**

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>ROM TESTED</th>
<th>CHECKSUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>6000</td>
<td>ROM0</td>
<td>02D9</td>
</tr>
<tr>
<td>9900</td>
<td>ROM1</td>
<td>0F0D</td>
</tr>
<tr>
<td>4000</td>
<td>ROM2</td>
<td>8265</td>
</tr>
<tr>
<td>6000</td>
<td>ROM3</td>
<td>17A9</td>
</tr>
<tr>
<td>0000</td>
<td>ROM4</td>
<td>E41F</td>
</tr>
<tr>
<td>0000</td>
<td>ROM5</td>
<td>55A7</td>
</tr>
<tr>
<td>0000</td>
<td>ROM6</td>
<td>B8E7</td>
</tr>
</tbody>
</table>

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