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COLOR X-Y POWER SUPPLY DIAGRAM

Notes:
- POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND), AND ONE WHITE WIRE (NEUTRAL).
- USE 4AMP 5A 250V FUSE AT FI WITH 220V AND 240V (EUROPEAN ONLY).

Gravitron Power Supply and Reg/Audio II PCB

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SP-206  Sheet 2A
1st printing
Gravitar™ PCB Schematic Diagram
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SP-206 Sheet 3B
1st printing
Test Connector

Address Decoder

Timing Diagram

NOTE: EITHER A 100K Ohm OR AN AMMETER MAY BE USED AT LOCATION D3. PIN NUMBERS NOT ENCLOSED IN PARENTHESES ARE FOR 100KOhm PIN NUMBERS IN PARENTHESES ARE FOR AN AMMETER.

Gravitar™ PCB Schematic Diagram

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SP-206 Sheet 4A 1/4 printing
Vector Data Shifters

Op Code and Intensity Latches

NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by are pulsing.
Adjusting X- and Y-Axis Video Potentiometers

If you replace the main Gravitar PCB or the display, you may have to make the following adjustments:

1. Enter self-test and advance to diagonal crosshatch pattern (Screen 2).

2. Centering Pots: Adjust X CENTER (R189) and Y CENTER (R212) so that the crosshatch pattern is located at the middle of the screen.

3. Size Pots: Adjust XSIZE (R192) and YSIZE (R213) so that the crosshatch pattern exactly covers the whole visible screen.

4. Linearity Pots: Adjust XLIN (R187) and YLIN (R210) so that the diagonal lines are straight. Since the LIN pots change the size of the displayed picture on the screen, you may have to readjust the SIZE pots in order to get the correct adjustment.

5. Bipolar Pots: Advance to the self-test raster pattern (Screen 4). Adjust XBIP (R99) and YBIP (R98) for a 1-inch high horizontal raster in the center of the screen. Be sure the raster ends are square with the sides of the outer rectangle.
Descriptions of Gravitar PCB Signal Names

A10, A13-A15
Address bits on Microprocessor Address Bus lines A10 and A13-A15 are generated by Microprocessor C2. Bits on lines A13-A15, together with those on A11-A12, are the input bits to Address Decoder R13. R13 is exclusive-Or'd with the A13-A15, by gate B6 to produce the A10 input bit for Random-Access Memory N1/P1.

Address bits A8-A9 are the select input signals for Address Decoder P3.

Address bits A11-A12 and A13-A15 are the input bits for Address Decoder R13 and addresses 1/2.

Address bits A8-A13 are applied with bits A8-A13 to Vector Address Selectors K6, M6, and N6 to pass the data lines on AM0-AM12.

Bits A8-A12 are control signals to custom audio chips B3 and C120 in the Option Switch Input and Audio Output circuit.

Bits A8-A18 are the input signals to latch P2 in the High-Score Table circuit where they are used to produce the A18 address input for EARROM M2.

A8
A8 is from A13, inverted by J3, and applied to Vector Address Selectors K8, when V8 is low, A8 and A13 select the specific memory Read-Only Memory.

AM0-AM13
Address bits on Multiplexed Address Bus lines AM0-AM13 are software-generated by Vector Address Selectors K8, L8, M8, and N8. When V8 is low, the Multiplexed Address Bus is from Buffered Microprocessor Address Bus A8 through AM12 and AM13. When V8 is high, AM0-AM12 is from Vector-Generator Address Bus lines AVGO-AVG13.

Signals AM0-AM12 are the input address signals to Vector Read-Only Memory L7, M7, N7, P7, and to Vector-Random Access Memory K7. In addition, AM11-A13 is the select input signals for Vector Address Decoders D2 and D13. Other signals for multiplexors N3 and R3 of the State Machine circuit.

AUD 1/2
The Audio 1 and Audio 2 signals are game PCB output signals that are generated by custom audio chips B3 and C12 in the Option Switch Input and Audio Output circuit. AUD 1 is the inverse of AUD 2. These signals are applied to the Audio Regulator T2 PCB and ultimately drive speakers 1 and 2.

AVGO-AVG13
Address bits on Vector-Generator Address Bus lines AVGO-AVG13 are software-generated by Vector Address Controller J8. When V8 is high, these signals are passed through the Vector Address Selectors on lines AM0-AM13 to the Vector-Read-Only Memory and the Vector-Random-Access Memory.

BANK SEL
The Bank Select signal is developed from line DB2. When latch R9 of the Coin Door and Control Panel Output circuit is clocked by latch Latch, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB8 to pin 9 of R9. From here, the signal is current amplified and inverted by Q2 and applied to the Right and Left Locate Coils of the game Coin Door.

BD0-DB7
Microprocessor Data Bus lines DB0-DB7 form a bi-directional data bus between the Microprocessor, the Read-Only Memory, and the Option Switch Input circuits.

DATA
Enable Disable is an active low level signal generated by test equipment connected to the DB DATA test point. DIS DATA is AND'd with the ROM signal by gate E3 to produce the enable signal for the Vector Random-Access Memory. When enable DIS DATA passes through Dislatch E2 passes data from the selected Read-Only Memory to the Microprocessor Bus.

DISLST
Display Reset is an active high level software-generated signal by latch 6 of the Halp Flag circuit. When either Reset or VGRST is input, latch 6 is set low. When DISLST resets C10, the State Machine latch K4, DAC Reference and Bipolar Current Sources latch E8, RG-B Output latch K10, Vector Scaling latch D7, Z Intensity and Blanking latch E6 and counter M3. In addition, DISLST resets the half-tone latch H5 low to the latch level high.

DOVGO-DVKY
Data bits on Vector-Generator Data Bus lines DVGO-DVKY are software-generated by the selected Vector Read-Only Memory or Vector Random Access Memory. If the Vector Memory Data Buffer latch is enabled (BUFFEN is low), the RWBV line is low, the data on lines DVGO-DVKY is passed through P8 to the Buffered Microprocessor circuit. Otherwise, the software-generated data on DVGO-DVKY is sent to the Vector Data Shifters and to the Op Code and Intensity Latches.

DVKY11-DVKY12
Data bits on X-Y game Vector Data Lines DVKX11-DVKX12 are software-generated by Vector Data Shifter A8, B8, C8, and by latch 95 of the Op Code and Intensity Latches circuit. DVKX11 and DVKX12 are the input signals to digital-to-analog converter A of the X-Axis Output circuit. The data on these lines changes from the current position of the display beam. If DVKX12 is low, DAC A/B operates only in its lower 512 positions, which means a negative direction of change on the display. If DVKX12 is high, DAC A/B operates only in its upper 512 positions for a positive direction of change on the display.

DVX0-DVX12
Data bits on Y-Axis Vector Data Lines DVX0-DVX12 are software-generated by Vector Data Shifter B8, H8, J8, and by latch 96 of the Op Code and Intensity Latches circuit. DVX0-DVX11 and DVX12 are the input signals for digital-to-analog converter DAC9 of the Y-Axis Output circuit. The data on these lines represents the Y-axis changes from the current location of the display beam. If DVX12 is low, DAC 9 operates only in its lower 512 positions, which means a negative direction of change on the display. If DVX12 is high, DAC 9 operates only in its upper 512 positions for a positive direction of change on the display.

DY0-DY12
Vector Data Bus lines DY0-DY12 form a buffered bi-directional data bus between microprocessor data buffer F2 and Vector Data Memory Buffer P8. Coin-Door and Control Panel Input latches buffer L9, M9, and N9. High-Score Table latches K2 and Z2; and High-Score Table buffer H2.

GAPPED
Blank is an active high-level signal generated by counter M3 in the Z Intensity and Blanking circuit and Orred with Z BLANK by gate M6 of the RG-B Output Circuit. When high, BLANK turns off Intensity latch E9, Q5, and Q6, which kills the RED, GREEN, and BLUE output signals to the display.

GROK
Coin Lockout is a game PCB output signal developed from the data on line DB9. When clocked by latch Latch, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB9 to pin 9 of R9. From here, the signal is current amplified and inverted by Q2 and applied to the Right and Left Locate Coils of the game Coin Door.

SIGNALS
When clocked by latch Latch, latch R9 of the Coin Door and Control Panel Output circuit, latches the data bit on DB5 to pin 5 of R9. From here, the signal is current amplified and inverted by Q2 and applied to the Coin Door or the game Coin Door.

STOP
STOP is an active high level signal generated by latch 95 of the Vector Data Shifter A8, B8, C8, and by latch 96 of the State Machine latch E6, which drives the Microprocessor. Other signals on the Coin Door and Control Panel Output circuit latch the data bit on DB10 to pin 10 of R9. From here, the signal is current amplified and inverted by Q2 and applied to the Game Utility Panel to actuate the Right Coin Counter.

Gravitar™ PCB Signal Name Descriptions
**Description of Gravitair PCB Signal Names (continued)**

**ENORM**

The active low-level Normalization Flag is software-generated by gate k4 of the Normalization Flag circuit. If D3 is high, A4 is high, and the output from gate J5 is high, ENORM is set low when STROBE goes high. If STROBE goes high, ENORM is reset to a low level when ENORM clears the 75 input pins of the Vector Data Shifters A4, B8, B9, F8, H8, and J8. ENORM is reset to a low level when ENORM clears the 75 input pins of the Vector Data Shifters (via shift left operations) at the same 2nd order specified by gate X18. (See Y16, V11, and V117 changes shown, which then sets ENORM to the high level.

**GO**

The Go flag is an active high-level signal software-generated by gate M5 of the Go Flag circuit when both STROBE and CNTR are high. GO is gated with HALT to gate N5 of the State Machine circuit to produce the A7 input address bit for State Machine ROM N4. GO is also used as the enable signal for Timer Block 0. When GO is high, the Timer Starter starts its count. The Timer Block counts to 256 if GO is high and D7 is low if GO is low and D7 is high, the Timer Block counts to 16K.

**GREEN**

Green is a game PCB output signal generated from the data line DTV1 in the RGB Output circuit. When DTV1 is high and latch K0 is clocked by STATLCH, the data line DTV1 is output and latched to pin 6 of K0. If both BLANK and 2 BLANK are active, this data line is also inverted by gate L10 to turn off the Blanking Block. A18 generates the GREEN signal for the display.

**HALT**

The active high-level Halt Flag signal is software-generated by latch L5 of the Halt Flag circuit. HALT is applied through buffer M9 of the Coin Door and Control Panel input circuit when (GSHI is low to allow Microprocessor C2 to reset the status of HALT on line D6B. In addition, HALT is applied to latch F4 of the State Machine circuit to develop HALT.

**HALT**

The active high-level Delayed Halt Flag signal is software-generated by latch L5 of the Delayed Halt Flag circuit. HALT is enabled when the HALT signal has been delayed by one pulse of the Inverted VGGC (-15 MHz, which in turn has been delayed by one pulse of 12 MHz. HALT is cleared with GO by gate N5 of the Inverter circuit used to produce the A7 input address bit for State Machine ROM N4.

**HALT**

The active low-level Halt Flag signal is software-generated by latch L5 of the Halt Flag circuit. HALT is the enable signal for Timer Block 0 latch E5 and Control Flag latch E6. In addition, HALT is output with CNTR by gate L5 of the Center Flag circuit to produce CENTER.

**INTACT**

Interrupt Acknowledge is an active low-level signal software-generated from Address Decoder P3 at address 8950. This signal is an acknowledgment from Microprocessor C2 that a interrupt request has been received. INTACT resets counter J4.

**INVERT X**

Invert X is an active high-level signal developed from the data pin on line D6B. When high, the Coin Door and Control Panel Output circuit latchs the data pin on D6B to pin 12 of N6. When low, INVERT X switches the buffer D10 through inverter E7 in the Y-Axis Output circuit. This inverts the X-axis vector instruction to the display.

**LATCH2**

Latch 2 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH2 is applied through inverter F7 to the S0 input pins of shift register A6B and B6 in the Vector Data Shifters circuit. LATCH2 causes the data bits on lines D2V0-D2V7 to be latched by A8 and C8 to lines D2V0-D2V7 when A8 is clocked by the 12-MHz clock signal.

**LATCH3**

Latch 3 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH3 is applied through inverter F7 to the S0 input pins of shift register B8 in the Vector Data Shifters circuit. LATCH3 causes the data bits on lines D2V0-D2V7 to be latched by B8 and C8 to lines D2V0-D2V7 when B8 is clocked by the 12-MHz clock signal.

**LATCH4**

LATCH4 is also the clock signal for Op Code and Intensity Latch 06. When LATCH4 goes low, the data bits on lines D2V0-D2V7 are latched by C8 to lines 2D24-D22, 2D17, and 2D12.

**NORM**

The active high-level Normalization Flag is software-generated by latch A6 in the Normalization Flag circuit. If D7 is high, the normalization flag is set high when STROBE goes high. NORM is gated with Scale and is set high when the Vector Timer Block 0 produces the load signal for the vector data shifters. When the Vector Timer Block 0 has been enabled, NORM initiates the divide-by-2 operation of the vector drawing time. (The factor of multiplication is by lines DTV0-DTV7 to Vector Scaling latch D7.)

**OPTION 2 OPTION 2**

The Option 0, Option 1, and Option 2 signals are hardware-generated by DIP switch D10. They are applied to shift input buffer D13 of the Coin Door and Control Panel Input Circuit. When L3 is enabled, these signals are passed to Buffered Microprocessor Data Lines DB6-DB7.

**OP1**

The Op 0 code signal is software-generated by latch D6 in the Op Code and Intensity Latch circuit. If the data on line DVS is high, OP1 is set when D6 is clocked by LATCH1. OP1 is multiplied with AMB by L3 in the State Machine circuit to produce the A6 input address bit for State Machine ROM N4.

**OP2**

The Op 2 code signal is software-generated by latch D6 in the Op Code and Intensity Latch circuit. If the data on line DVS is high, OP2 is set when D6 is clocked by LATCH1. OP2 is multiplied with AMB by L3 in the State Machine circuit to produce the A6 input address bit for State Machine ROM N4.

**OP3**

OP3, OP3, STROBE, and VGSC are all low, VCTRL from Vector Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal.

**OP4**

The OP4 code signal is software-generated by latch D6 in the Op Code and Intensity Latch circuit. If the data on line DVS is high, OP4 is low. If OP4 is low, it is applied through gates G7 and F3 to the Vector Scaling circuit as the load signal for counter 7. This allows the data fetched from DTV7:DTV0 by D7 to be loaded into counter 7. When STROBE goes high, counter 7 counts down until it reaches the minimum count. At the same time, the Timer Block 0 (divide-by-N) of the time circuit operates for each count of C7. (This is caused by SCALE being at the high level.) When C7 reaches its minimum count, it sets pin 12 high, dropping SCALE to the low state.

**OP5**

OP5 and DTV12 are low, SCALE, and SCALE is set low when STROBE goes low. This allows Vector Scaling latch D7 to latch the new data on DTV7:DTV0.

**OP6**

OP6, OP6, STROBE, and VGSC are all low. This allows latch E6 of the INT and Blanking circuit to latch the data on DTV4-DTV7.

**OP2**

The Complementary Op 0 code signal is software-generated by latch D6 in the Op Code and Intensity Latch circuit. This signal is opposite in state to OP2. If OP2, STROBE, and VGSC are low, CNTR from Center Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal. OP2 is also set high by gate R4 to produce the OP2 output signal for Vector Address Controller J8.

**OP6**

The Opposite Complementary Op 0 code signal is software-generated by latch D6 in the Op Code and Intensity Latch circuit. This signal is opposite in state to OP6. If OP6, STROBE, and VGSC are low, CNTR from Center Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal.

**Gravitair™ PCB Signal Name Descriptions**

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Description of Gravitar PCB Signal Names (continued)

**PORT 1 LED**
The Player 1 LED On signal is developed from the data bit on line DB4. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on line DB4 into pin 19 of R9. This signal is applied through R103 to light the Player 1 LED on the game Control Panel.

**PLAYER 2 LED**
The Player 2 LED On signal is developed from the data bit on line DB5. When clocked by latch R9, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB5 into pin 16 of R9. This signal is applied through R102 to light the Player 2 LED on the game Control Panel.

**PDR**
The active high-power-On Reset signal is hardware-generated at pin 4 of F7 in the Power-On Reset circuit. PDR is the clock signal that starts the count of 4 of the Clock circuit.

**PER**
The active high-power-On Reset signal is hardware-generated at pin 6 of Inverter F7 in the Power-On Reset circuit. PER is generated when the voltage at pin 3 of R6 is less than about 7 volts or when the RESET test point is shorted to ground. PER is developed into the RESET signal to protect Microprocessor C2.

**RAM**
The Random-Access Memory Enable is an active low signal, generated by Address Decoder R2 during addresses 0000 through 02FF. RAM is the chipenable signal for Random Access Memory N'P1. When low, RAM allows data to be read from or written to P'N1, depending upon the state of WRITE.

**RED**
Red is a game PCB output signal developed from the data line on D21Y in the R-B Output circuit. When D21Y is high and latch K10 is closed by STACLK, R-B is developed from latch 1 pin 5 of K10. Red and BLANK are low, allowing the data bit to be signaled via gate L10Q to turn on the RED. Transistor Q6 generates the RED signal for the display.

**RESET**
Reset is an active low-level signal generated at pin 5 of K3 from the Watchdog circuit. When the Watchdog circuit, the Power-On Reset circuit. The Watchdog reset circuit will set the active low level when the RESET test point is shorted to ground or during the time that the power-supply circuit is reaching its regulated levels. This ensures that the Microprocessor Address Bus is stabilized before the microprocessor begins operation.

The Watchdog circuit sets the active level to the low level when the microprocessor fails to output a value before Watchdog counter H'4 has reached its maximum count.

**RETURN**
Return is the clear signal for latch R9 in the Coin Door and Control Panel Output circuit. In addition, RETURN is gated with MG20 to gate L6 in the Hat Flag circuit to produce DISRT.

**ROM**
The Read-Only Memory Enable is an active high-level signal-generated from Address Decoder R1 during addresses 0000 through 00FF. ROM is enabled with I/O5 by gate R4 to enable bidirectional data bus F2 to pass data. In addition, ROM is ANDED with DIS RT to enable data buffer E2.

ROM0
Read-Only Memory Chip Select 0 or an active low-level signal, generated by Address Decoder R1 at addresses 0000-00FF. ROM0 is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, ROM0 allows ROM D1 to be addressed and to pass data to buffer E2.

ROM1
Read-Only Memory Chip Select 1 or an active low-level signal, generated by Address Decoder R1 at addresses 0001-000F. ROM1 is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, ROM1 allows ROM D1 to be addressed and to pass data to buffer E2.

ROM2
Read-Only Memory Chip Select 2 or an active low-level signal, generated by Address Decoder R1 at addresses 0002-00FF. ROM2 is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, ROM1 allows ROM D1 to be addressed and to pass data to buffer E2.

ROM3
Read-Only Memory Chip Select 2 or an active low-level signal, generated by Address Decoder R1 at addresses 0005-00FF. ROM2 is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, ROM1 allows ROM D1 to be addressed and to pass data to buffer E2.

ROM4
Read-Only Memory Chip Select 3 or an active low-level signal, generated by Address Decoder R1 at addresses 0006-00FF. ROM2 is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, ROM1 allows ROM D1 to be addressed and to pass data to buffer E2.

ROM5
Read-Only Memory Chip Select 3 or an active low-level signal, generated by Address Decoder R1 at addresses 0007-00FF. ROM2 is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, ROM1 allows ROM D1 to be addressed and to pass data to buffer E2.

ROM6
Read-Only Memory Chip Select 3 or an active low-level signal, generated by Address Decoder R1 at addresses 0008-00FF. ROM2 is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, ROM1 allows ROM D1 to be addressed and to pass data to buffer E2.

ROM7
Read-Only Memory Chip Select 3 or an active low-level signal, generated by Address Decoder R1 at addresses 0009-00FF. ROM2 is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, ROM1 allows ROM D1 to be addressed and to pass data to buffer E2.

ROM8
Read-Only Memory Chip Select 3 or an active low-level signal, generated by Address Decoder R1 at addresses 000A-00FF. ROM2 is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, ROM1 allows ROM D1 to be addressed and to pass data to buffer E2.

ROM9
Read-Only Memory Chip Select 3 or an active low-level signal, generated by Address Decoder R1 at addresses 000B-00FF. ROM2 is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, ROM1 allows ROM D1 to be addressed and to pass data to buffer E2.
Description of Gravitar PCB Signal Names (continued)

ST3  
State signal ST3 is an active high-level signal hardware-generated by Decoder Disable latch A7. ST3 is opposite in state at VCC, and is delayed by one pulse of the 12MHz clock signal if the Q4 output from State Machine ROM M4 is low and VEMEM is high. If the Q4 output from M4 is high, ST3 is high. When ST3 is high, State Machine decoder H7 is disabled. When ST3 is low, H7 decodes the data on lines ST0-ST2 to produce LATCHES-  LATCHES and STROBED-STROBE3.

VCRT, VCTR  
The Vector Flg signals are software-generated by Vector Flg latch ES, IF GPR, DPO, STROBED, and VCRT are low and VCRT is high, VCTR is set high and VCTR is set low when ES is clocked by the 12MHz clock signal. VCRT is OFFed with CTNHY by gate M5 to set GO high.

SCALE, CTNHY, DV111-DV112, and DV111-DV112 are gated with VCRT to produce the clear signal for Nomination Flag latch A6.

In the Z Intensity and Blanking circuit, VCTR is the clock signal for latch H6 and the serial input signal for shift register M3.

VCRT and VCTR are used by the DAC Reference and Bipolar Current Sources circuit to set the X BIP, Y BIP, X REF, and Y REF levels.

VGCK  
The Vector Generator clock signal is generated at pin 18 of buffer BI in the Microprocessor circuit. VGCK is derived from the 1.5 MHz clock signal and is applied to AND gate j5 of the State Machine Clock Logic circuit. VGCK is the basic timing signal of the State Machine circuit.

VGG0  
The Vector Generator Go signal is an active low-level signal software-generated by Address Decoder D9 at address 8840. VGG0 is the clear signal for latch L5 of the Halt Flag circuit. When low, VGG0 sets HALT to the inactive low level.

VGST  
The Vector Generator Reset is an active low-level signal software-generated by Address Decoder D9 at address 9680. VGST is OFFed by gate L6 of the Halt Flag circuit to produce DISRT.

VEMEM  
The Vector Memory Select Enable is an active low-level signal software-generated by Address Decoder D9 at address 2000 through 5FFF. VEMEM is the select-enable signal for Vector Address Selectors K5, L6, M6, and N8. When low, VEMEM allows the Vector Address Selectors to produce WI, BUFFEN, and the AM0-AM12 multiplexed address bits. VEMEM is also applied to gate K5 of the Vector Random-Access Memory Clock Logic circuit where it is used to generate ST3.

VRAM  
The Vector Random-Access Memory Chip Enable is an active low-level signal software-generated by Address Decoder D9 at address 2000-27FF. When low, VRAM enables Vector Random-Access Memory K7 to be addressed to display receive or transmit data, depending upon the state of VR VRAM is also used to produce the DAEEN signal from M5 of the Vector Address Selector circuit.

X OUt  
X OUt is a game PCB output signal generated by the X Axis Output circuit. X OUt carries the horizontal beam deflection signal for the drawing of vectors on the display.

X REF  
The X-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 10 of Axis digital-to-analog converter (DAC) A/89 of the X-Axis Output circuit.

Y BIP  
The Y-Axis Bipolar Current is set by R99 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pin 18 of Axis digital-to-analog converter (DAC) A/89 of the X-Axis Output circuit.

Y OUt  
Y OUt is a game PCB output signal generated by the Y Axis Output circuit. Y OUt carries the vertical beam deflection signal for the drawing of vectors on the display.

Y REF  
The Y-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of Axis digital-to-analog converter (DAC) F/9 of the Y-Axis Output circuit.

Z INT  
Z Intensity signals 20-ZZ and 21-ZZ are software-generated by latch C8 in the Op Code and Intensity Latches circuit. These signals are derived from the data on lines OCV1-DV7 when C8 is clocked by LATCH6. If the binary count carried by 20-ZZ is not equal to 1, these signals are the input signals for latch F6 in the Z Intensity and Blanking circuit. If the binary count carried by 20-ZZ is 1, Z Intensity signals 20-ZZ, 21-ZZ, and 22-ZZ are ANDed by gate F3 of the

Z INT and Blanking circuit to produce the select signal for latch F6. This select signal causes the latched data from F6 to be applied as the input signals for latch F6.

Z OUt  
Z Intensity Output is a game PCB output signal generated by the Z intensity and Blanking circuit from either DNY/DV7 or 20-ZZ. The Q output signals from latch H6 are summed at the base of Q7. Transistors Q7 and Q8 buffer Z OUt before it is sent to the game display circuitry to control the display intensity.

3 KHZ  
The 3 kHz clock signal is generated at pin 6 of Clock counter F4 and is applied through switch input buffer MS of the Coin Door and Control Panel input circuit (when SHJH is low). The 3 kHz clock is read by the microprocessor on data line D17. This frequency is the time reference for the Microprocessor C2.

12 KHZ  
The 12 kHz clock signal is generated at pin 4 of Clock counter F4 and is applied to reset A4 of the High Score Table.

3 MHz  
The 3 MHz clock signal is generated at pin 3 of Clock counter F4. The 3 MHz signal is ANDed with RWB and 942 by gate 24 to produce WRITE. It is also applied to AND gate 25 of the State Machine Clock Logic and to shift register M3 of the Z Intensity and Blanking circuit.

6 MHz  
The 6 MHz clock signal is generated at pin 3 of Clock counter F4 and is applied to gate 56 of the State Machine Clock Logic circuit.

12 KHZ  
The 12 kHz clock signal is generated at pin 10 of inverter F3 in the Clock circuit. This signal clocks the Vector Timer Shifters, the Vector Flag latch, and the Center Flag latch.
Troubleshooting with the Read/Write Controller

A. CAT Box Preliminary Set-Up
1. Remove the electrical power from the game.
2. Remove the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet.
4. Remove Microprocessor C2 from the game PCB.
5. Connect the harness from the game to the game PCB. (Use extenders, if available.)
6. Connect together the 40 and 42 test points on the game PCB with the shortest possible jumper.
7. Connect the WDDIS test point to ground.
8. Connect the CAT Box flex cable to the game PCB edge test connector.
9. Apply power to the game and to the CAT Box.
10. Set CAT Box switches as indicated:
   a. TESTER SEL-TEST: OFF
   b. TESTER MODE: R/W
   11. Press TESTER RESET.

B. Address Lines
1. Perform the CAT Box preliminary set-up.
2. Connect the DATA PROBE to the CAT Box.
3. Connect the DATA PROBE ground clip to a game PCB ground test point.
4. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. PULSE MODE: UNLATCHED
   c. R/W MODE: (OFF)
   d. R/W: WRITE
5. Key in the address pattern given in Table 1 (use AAAAAA to start) with the CAT Box keyboard.
6. Press DATA SET.
7. Key in the data pattern given in Table 1 (use AAAAAA to start) with the keyboard.
8. Set R/W MODE: STATIC.
9. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 1 lights up. Repeat this step for each IC-pin in Table 1.
10. Repeat parts 6 through 9 using address 5555 in part 5 and data 55 in part 7.

C. Data Lines
1. Perform the CAT Box preliminary set-up.
2. Connect the DATA PROBE to the CAT Box.

Table 1 Address Lines
<table>
<thead>
<tr>
<th>LOGIC STATE</th>
<th>IC-PIN</th>
<th>LOGIC STATE</th>
<th>IC-PIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R2:15</td>
<td>1</td>
<td>R2:15</td>
</tr>
<tr>
<td>0</td>
<td>R2:13</td>
<td>0</td>
<td>R2:13</td>
</tr>
<tr>
<td>1</td>
<td>R2:14</td>
<td>0</td>
<td>R2:14</td>
</tr>
<tr>
<td>1</td>
<td>R1:5</td>
<td>0</td>
<td>R1:5</td>
</tr>
<tr>
<td>1</td>
<td>B1:7</td>
<td>0</td>
<td>B1:7</td>
</tr>
<tr>
<td>0</td>
<td>B1:12</td>
<td>1</td>
<td>B1:12</td>
</tr>
<tr>
<td>0</td>
<td>B1:14</td>
<td>0</td>
<td>B1:14</td>
</tr>
<tr>
<td>1</td>
<td>B1:16</td>
<td>1</td>
<td>B1:16</td>
</tr>
<tr>
<td>1</td>
<td>C1:9</td>
<td>0</td>
<td>C1:9</td>
</tr>
<tr>
<td>0</td>
<td>C1:7</td>
<td>1</td>
<td>C1:7</td>
</tr>
<tr>
<td>0</td>
<td>C1:5</td>
<td>0</td>
<td>C1:5</td>
</tr>
<tr>
<td>1</td>
<td>C1:12</td>
<td>0</td>
<td>C1:12</td>
</tr>
<tr>
<td>1</td>
<td>C1:14</td>
<td>1</td>
<td>C1:14</td>
</tr>
<tr>
<td>1</td>
<td>C1:16</td>
<td>0</td>
<td>C1:16</td>
</tr>
<tr>
<td>0</td>
<td>C1:18</td>
<td>1</td>
<td>C1:18</td>
</tr>
</tbody>
</table>

3. Connect the DATA PROBE ground clip to the game PCB ground test point.
4. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. P/W MODE: (OFF)
   c. R/W: WRITE
5. Key in address 0000 with the keyboard.
6. Press DATA SET.
7. Key in data AA with the keyboard.
8. Set R/W MODE to PULSE and back to (OFF).
9. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 2 lights up. Repeat this check for each IC-pin in Table 2.
10. Repeat parts 6 through 9 using data 55 in part 7.

D. RAM
1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: ADDR
   b. BYTES: 1024
   c. R/W MODE: (OFF)
   d. R/W: WRITE
3. Enter address 0000 with the keyboard.
4. Set R/W MODE to PULSE and back to (OFF).
5. Set R/W: READ.
6. Set R/W MODE to PULSE and back to (OFF).
7. If the CAT Box reads an address that doesn’t compare with that written, the COMPARING ERROR LED will light up. The ADDRESS/SIGNATURE display of the CAT Box will show the failing address location and the ERROR DATA DISPLAY switch is enab-
ed. Using this switch, determine if the error is in the high-order or low-order RAM.
8. Repeat parts 2-d through 7 using addresses 0400, 2000, and 2400.
9. Repeat this test with DBUS SOURCE set to ADDR.

E. Custom Audio I/O Chips

Gravitar has two custom audio I/O chips. Each must be tested separately. There are several ways to test these chips:
- Perform the self-test.
- Substitute a known good part for a suspected defective part.
- Use the following procedure.

1. Perform the CAT Box preliminary set-up.

Table 2 Data Lines

<table>
<thead>
<tr>
<th>When writing</th>
<th>Data lines</th>
<th>When writing</th>
</tr>
</thead>
<tbody>
<tr>
<td>AA pattern</td>
<td>55 pattern</td>
<td>55 pattern</td>
</tr>
<tr>
<td>LOGIC STATE</td>
<td>IC-PIN</td>
<td>LOGIC STATE</td>
</tr>
<tr>
<td>1</td>
<td>F2-11</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>F2-12</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>F2-13</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>F2-14</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>F2-15</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>F2-16</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>F2-17</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>F2-18</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>F2-19</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>F2-20</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>F2-21</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>F2-22</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>F2-23</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>F2-24</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>F2-25</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>F2-26</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>F2-27</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>F2-28</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>F2-29</td>
<td>0</td>
</tr>
</tbody>
</table>

2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/W: WRITE
   c. R/W MODE: (OFF)
3. Enter the address from Table 3 with the keyboard.
4. Press DATA SET.
5. Enter the data from Table 3 with the keyboard.
6. Set R/W MODE to PULSE and back to (OFF).
7. Repeat parts 3 through 6 for each address and data listed in Table 3. Check for the response indicated.

Table 3 Custom Audio I/O Chips

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
<th>TEST RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>680F</td>
<td>00</td>
<td>Custom Audio I/O Chip B3 channel 1 produces pure tone.</td>
</tr>
<tr>
<td>680F</td>
<td>03</td>
<td>Custom Audio I/O Chip B3 channel 1 off.</td>
</tr>
<tr>
<td>6800</td>
<td>55</td>
<td>Custom Audio I/O Chip B3 channel 2 produces pure tone.</td>
</tr>
<tr>
<td>6801</td>
<td>AF</td>
<td>Custom Audio I/O Chip B3 channel 2 off.</td>
</tr>
<tr>
<td>6802</td>
<td>00</td>
<td>Custom Audio I/O Chip C3 channel 1 produces pure tone.</td>
</tr>
<tr>
<td>6803</td>
<td>AF</td>
<td>Custom Audio I/O Chip C3 channel 1 off.</td>
</tr>
<tr>
<td>6804</td>
<td>00</td>
<td>Custom Audio I/O Chip C3 channel 2 produces pure tone.</td>
</tr>
<tr>
<td>6805</td>
<td>03</td>
<td>Custom Audio I/O Chip C3 channel 2 off.</td>
</tr>
<tr>
<td>6806</td>
<td>55</td>
<td>Custom Audio I/O Chip C3 channel 3 produces pure tone.</td>
</tr>
<tr>
<td>6807</td>
<td>AF</td>
<td>Custom Audio I/O Chip C3 channel 3 off.</td>
</tr>
<tr>
<td>6808</td>
<td>00</td>
<td>Custom Audio I/O Chip C3 channel 4 produces pure tone.</td>
</tr>
<tr>
<td>6809</td>
<td>AF</td>
<td>Custom Audio I/O Chip C3 channel 4 off.</td>
</tr>
<tr>
<td>6810</td>
<td>00</td>
<td>Custom Audio I/O Chip C3 channel 5 produces pure tone.</td>
</tr>
<tr>
<td>6811</td>
<td>AF</td>
<td>Custom Audio I/O Chip C3 channel 5 off.</td>
</tr>
</tbody>
</table>

F. Player and Option Switch Inputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/W: READ
3. For each address listed in Table 4, do the following:
   a. Set R/W MODE to (OFF).
   b. Enter the address with the keyboard.
   c. Set R/W MODE to STATIC.
   d. Activate the input switch indicated in Table 4 for the address.

Table 4 Player and DIP Switch Inputs

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>INPUT SWITCH</th>
<th>TEST RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>7800</td>
<td>Right coin switch</td>
<td>Lower nybble (right digit) of DATA display changes when right or left coin, or self-test switches are activated. Upper nybble of DATA display is unstable.</td>
</tr>
<tr>
<td>8000</td>
<td>Player 1 SHIELDS, FIRE, ROTATE LEFT, ROTATE RIGHT, THRUST, START</td>
<td>Upper nybble of DATA display changes when each input switch is activated.</td>
</tr>
<tr>
<td>8800</td>
<td>Player 2 SHIELDS, FIRE, ROTATE LEFT, ROTATE RIGHT, THRUST, START</td>
<td>Upper nybble of DATA display changes when each input switch is activated.</td>
</tr>
</tbody>
</table>

G. Analog Vector-Generator

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. R/W: WRITE
   c. R/W MODE: (OFF)
3. Enter address 2000 with the keyboard.
4. Press DATA SET.
5. Enter the data from Table 5.
6. Set R/W MODE to PULSE and back to (OFF).
7. Repeat parts 4 through 6 for each address and data listed in Table 5 using the ADDRESS INCR button to advance the address by 1.

CAUTION
You may damage the circuitry of the X-Y display if you key in the VGGO signal without first checking all the addresses and data. Check the data by reading each address location using parts 8 through 11 below.

8. Set CAT Box switches as indicated:
   a. R/W: READ
   b. R/W MODE: (OFF)
9. Enter address or press ADDRESS INCR.
10. Set R/W MODE to PULSE.
11. Check the data shown in the DATA display against that listed in Table 5. If the data is correct, proceed with part 12.
12. Set CAT Box switches as indicated:
    a. R/W: WRITE
    b. R/W MODE: (OFF)
13. Enter VGG address 8840.
14. Set R/W MODE to PULSE and back to (OFF).
15. Check that the screen shows a large plus sign. Failure of the horizontal or vertical circuits shows up as a single line drawn on the screen. If the screen does not display a large plus sign, contact Atari Field Service.

### Table 6 LED and Coin Counter Outputs

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA 1</th>
<th>DATA 2</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0001</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0002</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0003</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0004</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0005</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0006</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0007</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0008</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0009</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0010</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0011</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0012</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0013</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0014</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0015</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0016</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>0017</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
</tbody>
</table>

**CAUTION**
If you write ON data to activate a solenoid, deactivate the solenoid immediately by writing the OFF data. If you leave a solenoid activated for more than 10 seconds, you may have to replace the solenoid and/or its driver, due to overheating.

4. For each DATA output listed in Table 5, do the following:
   a. To activate the output:
      • Press DATA SET.
      • Enter the ON data listed for the output.
      • Set R/W MODE to STATIC and back to (OFF).
   b. To deactivate the output:
      • Press DATA SET.
      • Enter the OFF data listed for the output.
      • Set R/W MODE to STATIC and back to (OFF).

### Table 7 Address Bus Signatures

<table>
<thead>
<tr>
<th>IC-PIN</th>
<th>SIGNAL NAME</th>
<th>SIGNATURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1-1</td>
<td>AB2</td>
<td>UUUU</td>
</tr>
<tr>
<td>C1-16</td>
<td>AB1</td>
<td>5555</td>
</tr>
<tr>
<td>C1-14</td>
<td>AB2</td>
<td>CCCC</td>
</tr>
<tr>
<td>C1-12</td>
<td>AB3</td>
<td>7777</td>
</tr>
<tr>
<td>C1-3</td>
<td>AB4</td>
<td>5454</td>
</tr>
<tr>
<td>C1-5</td>
<td>AB6</td>
<td>0450</td>
</tr>
<tr>
<td>C1-7</td>
<td>AB8</td>
<td>UPUP</td>
</tr>
<tr>
<td>C1-9</td>
<td>AB7</td>
<td>5454</td>
</tr>
<tr>
<td>B1-16</td>
<td>AB8</td>
<td>HC89</td>
</tr>
<tr>
<td>B1-14</td>
<td>AB9</td>
<td>2179</td>
</tr>
<tr>
<td>B1-12</td>
<td>AB10</td>
<td>HP90</td>
</tr>
<tr>
<td>B1-7</td>
<td>AB11</td>
<td>1223</td>
</tr>
<tr>
<td>B1-5</td>
<td>AB12</td>
<td>H97P</td>
</tr>
<tr>
<td>R2-12</td>
<td>A13</td>
<td>3395</td>
</tr>
<tr>
<td>R2-13</td>
<td>A14</td>
<td>3297</td>
</tr>
<tr>
<td>R2-14</td>
<td>A15</td>
<td>755U</td>
</tr>
</tbody>
</table>

### Troubleshooting with Signature Analysis

#### A. Signature Analysis Set-Up
1. Perform the CAT Box preliminary set-up.
2. Connect the three BNC-to-EZ clip cables supplied with CAT Box to the SIGNATURE ANALYSIS CONTROL, START, STOP, and CLOCK jacks of the CAT Box.
3. Connect the three black EZ clips to a game PCB ground test point.
4. Connect the CAT Box DATA PROBE to the DATA jack on the CAT Box.
5. Set the CAT Box switches as indicated:
   a. TESTER MODE: SIG
   b. TESTER SELF-TEST: OFF
   c. R/W MODE: LATCHED
   d. START: Negative-going edge trigger
   e. STOP: Negative-going edge trigger
   f. CLOCK: Negative-going edge trigger

#### B. Address Lines
1. Perform the signature analysis set-up.
2. Connect the START probe tip to pin 14 of IC R2.
3. Connect the STOP probe tip to pin 14 of IC R2.
4. Connect the CLOCK probe tip to 42 test point on the game PCB.
5. Verify the set-up connections by connecting the DATA PROBE to a game PCB ground test point. The CAT Box ADDRESS/SIGNATURE display should show 0000. Now connect the DATA PROBE to a +5V test point; the ADDRESS/SIGNATURE display should show 0001.

#### C. Address Decoder

**CAUTION**
While testing decoders and ROMs, adding 270 pF capacitors to A12, A13, A14, and A15 may be necessary to eliminate unstable signatures.

1. Perform parts 1 through 5 of the address bus signature procedure.
2. Probe the IC-pin listed in Table 8 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC-pin listed.

---

### Table 8 Decoder Signatures

<table>
<thead>
<tr>
<th>IC-PIN</th>
<th>SIGNAL NAME</th>
<th>SIGNATURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>R2-1</td>
<td>RAM</td>
<td>3APF</td>
</tr>
<tr>
<td>R2-2</td>
<td>ROM</td>
<td>593H</td>
</tr>
<tr>
<td>R2-3</td>
<td>ROM</td>
<td>53H6</td>
</tr>
<tr>
<td>R2-4</td>
<td>ROM</td>
<td>96F9</td>
</tr>
<tr>
<td>R2-5</td>
<td>ROM</td>
<td>942F</td>
</tr>
<tr>
<td>R2-6</td>
<td>ROM</td>
<td>3PCF</td>
</tr>
<tr>
<td>R2-7</td>
<td>ROM</td>
<td>3PCF</td>
</tr>
<tr>
<td>R2-8</td>
<td>ROM</td>
<td>942F</td>
</tr>
<tr>
<td>R2-9</td>
<td>ROM</td>
<td>84AF</td>
</tr>
<tr>
<td>R1-1</td>
<td>VMEM</td>
<td>95U3</td>
</tr>
<tr>
<td>R1-2</td>
<td>ROM</td>
<td>942F</td>
</tr>
<tr>
<td>R1-3</td>
<td>ROM</td>
<td>743H</td>
</tr>
<tr>
<td>R1-4</td>
<td>ROM</td>
<td>743H</td>
</tr>
<tr>
<td>R1-5</td>
<td>ROM</td>
<td>743H</td>
</tr>
<tr>
<td>R1-6</td>
<td>ROM</td>
<td>743H</td>
</tr>
<tr>
<td>R1-7</td>
<td>ROM</td>
<td>743H</td>
</tr>
<tr>
<td>R1-8</td>
<td>ROM</td>
<td>743H</td>
</tr>
<tr>
<td>R1-9</td>
<td>ROM</td>
<td>743H</td>
</tr>
</tbody>
</table>

### Watchdog Troubleshooting

The Watchdog circuit will send continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuitry. If the self-test fails to run, it is a good practice to check the reset line. A pulsing RESET line indicates that something is causing the microprocessor to lose its place in the program. Typical causes are:
1. Open or shorted address or data bus lines.
2. Bad microprocessor chip.
3. Bad bus buffers.
4. Bad ROM.
5. Bad RAM.
6. Any bad input or output that causes an address or data line to be held in a constant high or low state.

A pulsing RESET signal indicates a problem exists somewhere within the microprocessor circuitry rather than within the analog vector-generator.