Drawing Package Supplement

to

Centipede™

Operation, Maintenance and Service Manual

Contents of this Drawing Package

Game Coin Door and Power Supply Wiring Diagram
Microprocessor, Signature Analysis Procedure, Sync Generator, CAT Box™, and Power Inputs
Playfield Address Selector, Playfield Memory and Playfield Code Multiplexer
Coin Door Inputs, Switch Inputs, Video Outputs and Trak Ball™ Circuitry

Sheet 1, Side A
Sheet 1, Side B
Sheet 2, Side A
Sheet 2, Side B
Regulator Audio II PCB

The Regulator/Audio II PCB has been designed to filter and amplify the +5 VDC logic power to drive the audio circuit from the game PCB.

Regulator Circuit

The regulator consists of high performance component sets that pass transistor Q3 and Q3's driver circuit. The regulator accurately regulates the logic power supplied to the game PCB by monitoring the voltage through the +5VDC and ground inputs to the regulator. The presence of the +5 VDC and ground inputs to the regulator enables the regulator to effectively eliminate any voltage drops or voltage offset at the point where the harness between the regulator and the actual regulator output (ground) is connected. Resistor R8 is adjusted for the correct voltage gain. Once adjusted, the voltage at the input should remain constant at this voltage.

Regulator Adjustment

1. Connect a voltmeter between +5 VDC and ground of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio II PCB for +5 VDC reading on the regulator.
3. Connect a voltmeter between the regulator and the game PCB. Voltage drop should be less than +0.5 VDC. If it is higher, replace connectors on both the game and Regulator/Audio II PCB.
4. If cleaning PCB edge connectors, power off and remove edge connector, apply a voltage difference, connect minus lead of a test point to the Regulator/Audio II test point or GND test point of game PCB.

Now connect minus lead of -VDC on Regulator/Audio II test point on game PCB. From the edge connector, amplifier harness circuit is dropping the -VDC from the appropriate harness wire connection.

Audio Circuit

The audio circuit contains two integrated amplifiers. Each amplifier consists of a single-transistor amplifier with an effective gain of 2.2.
dual functions of regulating game PCB and amplifying audio.

regulator Q1, power resistor Q2. The regulator input to the game with high-impedance inputs are directly from the game PCB. Therefore, the game PCB. This IR loss in the wire to the game PCB. Variable DC on the game PCB. Variable DC on the game PCB. Variable DC on the game PCB.

and GND test points of the Regulator/Audio II

V REG and GND on a voltmeter. Use edge of voltmeter to GND PCB and plus lead to test voltage.

doesn't decrease voltage. Use voltmeter to +5 V test and plus lead to +5 V as you can see which is a test point. Troubleshoot harness connector.

dependent audio amplifier 2002AV amplifier with

American-Made Company
## Diagnostic Tests

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Use of Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Hold the slam switch closed, while setting the self-test switch to the on position.</td>
<td>The monitor displays the color hue adjustment pattern of 16 rectangles, as follows. Do not attempt any color hue or brightness adjustments unless you are a qualified color TV technician!</td>
</tr>
<tr>
<td>Pale Yellow-Green</td>
<td>Orange</td>
</tr>
<tr>
<td>Light Green</td>
<td>Dark Green</td>
</tr>
<tr>
<td>Deep Rose</td>
<td>Red</td>
</tr>
<tr>
<td>Navy Blue</td>
<td>Black</td>
</tr>
<tr>
<td>2. Activate any of the coin switches on the coin door.</td>
<td>A convergence pattern appears with a grid of white dots on a black screen. Do not attempt any convergence adjustments unless you are a qualified color TV technician!</td>
</tr>
<tr>
<td>3. Set self-test switch to the <strong>off</strong> position.</td>
<td>Check attract-mode display and readjust brightness if necessary.</td>
</tr>
</tbody>
</table>

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Sheet 1, Side B

Centipede™

Synchronizer

Signature Analysis Procedure

CAT Box™ Preliminary Set-Up

Power Input

Microprocessor

Address Decoder

RAM

ROM

Memory Map

Section of 037241-01 B

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Power Input

Testing the CAT Box

1. Perform the CAT Box CHECKOUT.

2. Set the CAT Box to 0000/1000.
   a. Press TEST1.
   b. DBUS SOURCE.
   c. BYTES to 1000.
   d. R/W MODE.
   e. R/W to WRITE.
   f. Key in 0000.
   g. Toggle R/W.
   h. R/W to READ.
   i. Toggle R/W.

3. If the CAT Box shows COMPARE ERROR, repeat the test.

4. If the COMPARE ERROR persists, repeat the test with a new sample to ensure the CAT Box is good.
A preliminary setup:

- DE to SINGLE
- PRESET
- ADR
- LED does not light, rekey 0000 and re-check Address.

Address location, and the ERROR DATA.

The DBUS SOURCE switch set to ADDR. This

is displayed.

The LED does not light after this step, the RAM

is displayed.

san address that doesn't compare the COM.
### Memory Map

<table>
<thead>
<tr>
<th>HEXA-DEcimal Address</th>
<th>R/W</th>
<th>DATA</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000-03FF</td>
<td></td>
<td>D D D D D D D D</td>
<td>RAM</td>
</tr>
<tr>
<td>0400-07BF</td>
<td></td>
<td>D D D D D D D D</td>
<td>Playfield RAM</td>
</tr>
<tr>
<td>07CC-07CF</td>
<td></td>
<td>D D D D D D D D</td>
<td>Motion Object Picture</td>
</tr>
<tr>
<td>07DD-07DF</td>
<td></td>
<td>D D D D D D D D</td>
<td>Motion Object Vert.</td>
</tr>
<tr>
<td>07E0-07EF</td>
<td></td>
<td>D D D D D D D D</td>
<td>Motion Object Horiz.</td>
</tr>
<tr>
<td>07F0-07FF</td>
<td></td>
<td>D D D D D D D D</td>
<td>Motion Object Color</td>
</tr>
<tr>
<td>0800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Option Switch 1 (0 = On)</td>
</tr>
<tr>
<td>0801</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Option Switch 2 (0 = On)</td>
</tr>
<tr>
<td>0C00</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Horizontal Trak Ball™ Inputs</td>
</tr>
<tr>
<td>0C01</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>VBLANK (1 = VBlank)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Self-Test (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Cocktail Cabinet (1 = Cocktail)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D</td>
<td>R,C,L Coin Switches (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D</td>
<td>SLAM (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Player 2 Fire Switch (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Player 1 Fire Switch (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Player 2 Start Switch (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Player 1 Start Switch (0 = On)</td>
</tr>
<tr>
<td>0C02</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Vertical Trak Ball™ Inputs</td>
</tr>
<tr>
<td>0C03</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Player 1 Joystick (R, L, Down, Up)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D</td>
<td>Player 2 Joystick (0 = On)</td>
</tr>
<tr>
<td>1000-100F</td>
<td>R/W</td>
<td>D D D D D D D D</td>
<td>Custom Audio Chip</td>
</tr>
<tr>
<td>1404</td>
<td>W</td>
<td>D D D D D D D D</td>
<td>Playfield Color RAM</td>
</tr>
<tr>
<td>140C</td>
<td>W</td>
<td>D D D D D D D D</td>
<td>Motion Object Color RAM</td>
</tr>
<tr>
<td>1600</td>
<td>W</td>
<td>D D D D D D D D</td>
<td>EA ROM Address &amp; Data Latch</td>
</tr>
<tr>
<td>1680</td>
<td>W</td>
<td>D D D D D D D D</td>
<td>EA ROM Control Latch</td>
</tr>
<tr>
<td>1700</td>
<td>W</td>
<td>D D D D D D D D</td>
<td>EA ROM Read Data</td>
</tr>
<tr>
<td>1800</td>
<td>W</td>
<td>D D D D D D D D</td>
<td>IRQ Acknowledge</td>
</tr>
<tr>
<td>1C00</td>
<td>W</td>
<td>D D</td>
<td>Left Coin Counter (1 = On)</td>
</tr>
<tr>
<td>1C01</td>
<td>W</td>
<td>D D</td>
<td>Center Coin Counter (1 = On)</td>
</tr>
<tr>
<td>1C02</td>
<td>W</td>
<td>D D</td>
<td>Right Coin Counter (1 = On)</td>
</tr>
<tr>
<td>1C03</td>
<td>W</td>
<td>D D</td>
<td>Player 1 Start LED (0 = On)</td>
</tr>
<tr>
<td>1C04</td>
<td>W</td>
<td>D D</td>
<td>Player 2 Start LED (0 = On)</td>
</tr>
<tr>
<td>1C07</td>
<td>W</td>
<td>D D</td>
<td>Trak Ball™ Flip Control (0 = Player 1)</td>
</tr>
<tr>
<td>2000</td>
<td>W</td>
<td>D</td>
<td>WATCHDOG</td>
</tr>
<tr>
<td>2400</td>
<td>W</td>
<td>D</td>
<td>Clear Trak Ball™ Counters</td>
</tr>
<tr>
<td>2000-3FFF</td>
<td>R</td>
<td></td>
<td>Program ROM</td>
</tr>
</tbody>
</table>
**Signature Analysis Procedure**

1. Perform the CAT Box™ preliminary set-up.

2. Connect the three BNC to E-Z clip cables (supplied with the CAT Box) to the SIGNATURE ANALYSIS CONTROL START, STOP, AND CLOCK jacks on the CAT Box.

3. Attach the three black E-Z clips to a ground loop on the CENTIPEDE™ game PCB.

4. Attach the CAT Box data probe to the DATA jack on the CAT Box.

5. The red E-Z clips on the cables will be moved about for each group of signatures to be taken. The set-up for each group of signatures is located on the schematic sheet near the device to be checked. The signatures are located on or near the signal point on the schematic.

   Note the example:  
   
<table>
<thead>
<tr>
<th>IC#</th>
<th>PIN#</th>
<th>SET-UP</th>
<th>START</th>
<th>SLOPE</th>
<th>STOP</th>
<th>CLK</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>P2</td>
<td></td>
<td>P2</td>
<td>N1</td>
</tr>
</tbody>
</table>

6. Set the CAT Box switches as follows:
   a. TESTER MODE: SIG
   b. TESTER SELF TEST: OFF
   c. PULSE MODE: LATCHED
   d. START:
   e. STOP:
   f. CLOCK:
Preliminary Set-up

1. Power from the game.
2. Connect the stand lead from the game PCB.
3. Connect cables to the game PCB and the wiring harness.
4. Connect the MPU socket with a piece of 28 AWG wire.
5. Connect the cable to the game PCB test edge connector.
TEST CONNECTOR—FOR ATARI CAT BOX™

Microprocessor

To Sheet 2, Side B
Sheet 2, Side A

Centipede™

Playfield Address Selector
Playfield Memory
Playfield Multiplexer
Picture Data ROM Circuitry
Motion Object Circuitry (Vertical)
Motion Object Circuitry (Horizontal)

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from the corporation.
The Motion Object Circuitry (vertical) receives playfield data and sync generator circuitry to generate the vertical component of the motion object. The output is gated by A7 when a motion object is on one of the six 15 from the playfield memory and 1V-128V from the sync generator area. The output is latched by E6 to AND gate B7. A low on B7 pin 8 indicates the presence of one of the vertical lines during non-active video time. This signal (M1) is passed to complexers in the picture data circuitry.

When 256H on pin 1 of D7 goes high, 1V, 2V, 4V and PIC0 are selected to the latched output of E6 is selected. The output of D7 is EXCLUSIVE OR sent to the picture data selector circuitry as motion graphic address or input to EXCLUSIVE OR gate E7 is PIC7 from the playfield code memory when high causes the output of E7 to be complimented. For example, PIC7 causes MGA0-MGA3 to go high. This causes the motion object to pass from Sync Generator Sheet 1, Side B.
Motion Object Circuitry (Horizontal)

The motion object circuitry (horizontal) receives playfield data and horizontal sync generator circuitry. PFD16-PFD23 from the playfield memory determine the position of the motion object. PFD24-PFD29 from the playfield memory determine the color of the motion object. PFD16-PFD23 are latched by L7 and loaded into the horizontal counters A5 and B5 by a low on pin 9. The horizontal position counters then RAMs A6 and B6. These RAMs are loaded with the video data for the particular RAMs from shift registers H9 and J9 (which were loaded from the graphics ROM). The RAMs A6 and B6 is then sent to the color PROM circuitry as MR0 and MR1.
Horizontal)

The horizontal and vertical inputs from the memory determine the horizontal and vertical position of the objects. The counters then address the particular motion object (from the motion object ROM) to the playfield code multiplexer, MGA0-MGA3 (motion graphics address) from the motion object circuitry, 256H and 256F from the sync generator. PICO-PIC5 represent the code for the object to be displayed. MGA0-MGA3 set one of eight different combinations of the 8-line by 8-bit blocks of picture video or the 16 line by 8 bit blocks of motion object video.

256H when high selects the playfield picture color codes to be addressed, 256F when low selects the motion object color codes to be addressed. The picture data ROM output D1-D8 on F7 and H/J7 are multiplexed by F6, H8, J8 and K8 and shifted out serially at H9 and J9. This serial output is latched by F9 as AREA0 and AREA1 to the motion object horizontal circuitry and the video output circuit.
Centipede Player-2000

Testing the Playfield Address Selector

1. Perform the CAT Box test.

2. Set the CAT Box switches:
   a. Press TESTER 1.
   b. DBUS SOURCE.
   c. BYTES TO 1024.
   d. R/W MODE to "0".
   e. R/W to WRITE.
   f. Key in 0400.
   g. Set R/W MODE to "1".
   h. R/W to READ.
   i. Set R/W MODE to "0".

Playfield Address Selector

The Playfield Address Selector controls the access to the playfield memory. It allows either the game MPU or the sync generator to scan the playfield memory. The Playfield Address Selector consists of multiplexers P5, and P7 and gate K4.

When \( 4H \) on pin 1 of P5 and P7 is low and pin 15 on P7 is low, the Playfield Address Selector receives 8H, 16H, 32H, and 64H on P5 and 16V, 32V, 64V, and 128V on P7 from the sync generator. These signals enable the sync generator circuits to access the playfield memory.

When \( 4H \) goes high the game MPU addresses the playfield memory (via AB0-AB9) for the positioning of the graphics. During horizontal blanking (pin 15 of P7 is high) the outputs of P7 (PFA4-PFA7) are held high enabling the motion object circuitry to access the playfield memory for the motion objects to be displayed.
3. If the CAT Box reads an address that doesn't compare, the COM-
    PARE ERROR LED lights, the ADDRESS/SIGNATURE display
    shows the failing address location, and the ERROR DATA DIS-
    PLAY switch is enabled.

4. If the COMPARER ERROR LED does not light, rekey 0400 and re-
    peat the test with the DBUS SOURCE switch set to ADDR. This
    ensures that the data bits at address 0400 will go high. If the
    COMPARER ERROR LED does not light after this step, the Play-
    field RAM is good.
Playfield Multiplexer

- Multiplexer receives playfield data from the playfield memory and the output (PF0-PF7) is a code that determines what is 1) display, or 2) read or updated by the MPU. The Playfield Multiplexer controls multiplexers K6, L6, M6, N6 and P6.

- 0H and 4H is high, AB4 and AB5 from the MPU address bus is the address from P6. This output is applied to multiplexers K6, L6, M6, and N6 inputs. When the MPU is accessing the playfield code multiplexer, the bits from the sync generator (128H and 8V) are the selected outputs. When the MPU reads the playfield codes, the select which bits of data PFD0-PFD31 are sent out via K6, L6, M6, N6, the playfield codes that eventually are displayed on the monitor.

- The codes (PF0-PF7) are latched by J5 and J6 to the MPU data bus (J5) and data PROM circuitry (J6). When the MPU reads, 1H from the MPU data bus go low, the inputs on J5 (PF0-PF7) are latched out to the MPU via J6 on pin 11 of J6 goes high, the inputs (PF0-PF7) are latched to the OM circuitry.
Picture Data ROM Circuitry

The picture data ROM circuitry receives picture information, assigns a color code to the information and sends it to the color PROM circuitry. The picture data ROM circuitry consists of ROM devices F7 and H/J7, multiplexers F8, H8, J8, K8, shift registers H9 and J9, and latch F9.
Testing the Option Switches

1. Perform the CAT Box preliminary set-up.

2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/W to READ
   d. Key in address 0800 (N9) or 0801 (N8)
   e. R/W MODE to STATIC

3. Activate the switch while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the switch is operating properly.

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Sheet 2, Side B

Centipede™

Joystick Circuitry
Mini-Trak Ball™ Circuitry
Player Input Circuitry
Video Output Circuitry
Audio Output Circuitry
Coin Counter Output Circuitry
Option Input Circuitry
High Score Memory Circuitry

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Coin Counter Output Circuit

This circuit consists of coin counter drivers Q6, Q7, and Q8 and data latch M10. The circuit is addressed by the MPU on ABO-AB2 and written by the MPU on data line DB7. When the input to a driver is clocked high, its collector goes low grounding the return of the coin counter in the coin door.

Mini-Trak Ball™ Circuitry

Testing the Mini-Trak Ball™ Inputs

1. Perform the CAT Box Preliminary Set-up.

2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/W to READ
   d. Key in address 0C00 (vertical) or 0C02 (horizontal)
   e. R/W MODE to PULSE

3. Spin the Mini-Trak Ball™ while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the Mini-Trak Ball input is operating properly.
1. If A8 pin 11 is low, transistor Q5 conducts and draws current from COLOR 3. The result is a pale blue when COLOR 1 and COLOR 2 are off.

2. If A8 pin 10 is low, transistor Q4 conducts and draws current from COLOR 2. The result is a pale green when COLOR 1 and COLOR 3 are off.

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**High Score Memory Circuitry**

The High Score Memory circuit stores the three best scores and other pertinent information. These scores are saved even if power is removed from the game. The High Score Memory circuit consists of an erasable reprogrammable ROM E5, latches E4, H4, J4, buffer H5 and timer A11.

A11 produces a 0-15V square wave at a 1V rate. This signal, when +15V, forward biases diode CR5 and allows capacitor C86 to charge to -29V. When the signal is 0V, CR5 is cutoff and CR4 is forward biased which causes C84 to develop a charge. C84 charges to approximately -28V. This is the potential required for EAROM C0 to operate.

The MPU addresses the EAROM (AB0-AB5) when a low EAADDR gates WRITE2 at gate A4. The trailing edge of the gated pulse latches the address information to the EAROM E5 via J4. Data is latched by H4 at the same time. The EAROM mode (read, write or erase) is determined by DB0-DB3 at latch E4. A low EACONTROL gates WRITE2 at gate A4. The trailing edge of this gated pulse latches the data into the EAROM E5 via latch H4.

Data is read from the EAROM when EAREAD on pin 1 of buffer H4 goes low.
Joystick Circuitry

Option Input Circuitry
Testing the Player Inputs

1. Perform the CAT Box Preliminary set-up.

2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/W to READ
   d. Key in address 0C00 (self-test switch only) or 0C01 (all others).
   e. R/W MODE to STATIC

3. Activate the following player input switches, one at a time, while monitoring the DATA DISPLAY:
   a. Coin Right
   b. Coin Left
   c. SLAM
   d. FIRE
   e. START 1
   f. START 2

4. The DATA DISPLAY will change if the switches are operating properly.

Denotes a test point

Testing the Audio Outputs

1. Perform the CAT Box preliminary set-up.

2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/W to WRITE
   d. Key in address or press ADDRESS INCR
   e. Press DATA SET
   f. Key in data
   g. Set R/W MODE to PULSE, then to OFF.
   h. For each address, repeat sequence starting at Step d.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
<th>RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>100F</td>
<td>00</td>
<td>Pure tone is heard from channel 1 output.</td>
</tr>
<tr>
<td>100F</td>
<td>03</td>
<td>Channel 1 output is turned off.</td>
</tr>
<tr>
<td>1000</td>
<td>55</td>
<td>Pure tone is heard from channel 2 output.</td>
</tr>
<tr>
<td>1001</td>
<td>AF</td>
<td>Channel 2 output is turned off.</td>
</tr>
<tr>
<td>1001</td>
<td>00</td>
<td>Pure tone is heard from channel 3 output.</td>
</tr>
<tr>
<td>1002</td>
<td>55</td>
<td>Channel 3 output is turned off.</td>
</tr>
<tr>
<td>1003</td>
<td>AF</td>
<td>Pure tone is heard from channel 4 output.</td>
</tr>
<tr>
<td>1003</td>
<td>00</td>
<td>Channel 4 output is turned off.</td>
</tr>
<tr>
<td>1003</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>1005</td>
<td>AF</td>
<td></td>
</tr>
<tr>
<td>1005</td>
<td>00</td>
<td></td>
</tr>
<tr>
<td>1006</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>1007</td>
<td>AF</td>
<td></td>
</tr>
<tr>
<td>1007</td>
<td>00</td>
<td></td>
</tr>
</tbody>
</table>

The video output circuit receives motion object, playfield, address and data inputs and produces a video output to be displayed on the game monitor. In order to read out of the color RAM, GRY0 and GRY1 from the motion object circuitry are multiplexed with AREA0 and AREA1 from the playfield circuit by EB. The output, selected by GRY0 or GRY1, is RAMA0-RAMA3 (RAM ADDRESS).

RAMA0-RAMA3 are applied to color RAM C8. The colors red, green, blue and an alternate color bit are outputs. The three color bits are latched by A8 as the game video in the three basic colors (or shades of gray in a black and white monitor). When the alternate color bit (C8 pin 11) is active, an alternate shade of blue or green is available.

The following conditions, along with the various combinations of COLOR 1 (red), COLOR 2 (green) and COLOR 3 (blue),