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**Schematic Package Supplement to**

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**Operators Manual**

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**ATARI**

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</tr>
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<td>D000-DFFF</td>
<td>R</td>
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<td>ROM 4</td>
</tr>
<tr>
<td>C000-CFFF</td>
<td>R</td>
<td>D D D D D D D D</td>
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<tr>
<td>B000-BFFF</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>ROM 6</td>
</tr>
<tr>
<td>A000-AFFF</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>ROM 7</td>
</tr>
<tr>
<td>9000-9FFF</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>ROM 8</td>
</tr>
<tr>
<td>8800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>CABINET 1</td>
</tr>
<tr>
<td>8800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>START 2</td>
</tr>
<tr>
<td>9800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>START 1</td>
</tr>
<tr>
<td>8900</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>SPARE</td>
</tr>
<tr>
<td>8900</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>FIRE UP</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>FIRE DOWN</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>FIRE LEFT</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>FIRE RIGHT</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>INVERT 2</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>INVERT 1</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>PLAY 1 LED</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>PLAY 2 LED</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>COIN LOCKOUT</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>BANK SEL</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>COIN CNTRL</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>COIN CNTR R</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>3KHZ</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>HALT</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>SEL.TEST</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>COIN AUX</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>COIN L</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>COIN R</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>E2ROMD</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>I/O01</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>I/O08</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>VROM 3</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>VROM 2</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>VROM 1</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>VROM 0</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>VROM</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>RAM</td>
</tr>
<tr>
<td>7800</td>
<td>R</td>
<td>D D D D D D D D</td>
<td>RAM</td>
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Descriptions of Black Widow Printed Circuit Board Names

A10, A13-A15
Address bits on Microprocessor Address Bus lines A10 and A13-A15 are generated by Microprocessor C2. Bits on lines A13-A15 are ORed together. Bits on lines A10, A11, and A12 are the input bits to Address Decoders R1-R2. A10 is exclusive-Orred with BANK SEL by gate 96 to produce the A10 input bit for Random-Access Memory N/P1.

AB0-AB12
Address bits on Buffered Microprocessor Address Bus lines AB0-AB12 are software-generated by Microprocessor C2 and buffered by B1 and C1. These signals are Random-Access Memory Memories D1, E1/F1, H1, J1, K1/L1, and M1; and to Random-Access Memory N/P1. Address bits AB6-AB8 are the select input signals for Address Decoder P3. Address bits AB11-AB12 and AB13-A15 are the input bits for Address Decoder R1 and R2. Address bits AB0-AB13 are applied with bits from AVG0-AVG12 to Vector Address Selector KS8, KS6, KS8, and KB6 to produce the data lines on Lines AM0-AM12.

Bits AB0-AB5 are control signals to custom audio chips B3 and C0/D3 in the Option Switch Input and Audio Output circuit. Bits AB6-AB8 are the input signals to latch P2 in the High-Score data table circuit where they are used to produce the A14-A15 address input for EAROM M2.

AB3
AB3 is from AB13, inVERTed by J3, and applied to Vector Address Selector M6. When VME is low, AB3 and AB13 select the specific Vector Memory Read-Only Memory.

AM0-AM12
Address bits on Multiplexed Address Bus Lines AM0-AM12 are software-generated by Vector Address Selectors KS8, KS6, KB6, and KB8. When VME is low, the Multiplexed Address Bus is from Buffered Microprocessor Address Bus AB0 through AB12 and AB13. When VME is high, AM0-AM12 is from Vector-Address Generator Bus Lines AVG0-AM12. Signals AM0-AM11 are the input address signals to Vector Read-Only Memory L7, M7/N7, N7/P7, and to Vector Random-Access Memory K7. In addition, AM11-AM12 are the select input signals for Vector Address Selector KS6. Signals AM0-AM12 are used for multiplexors N3 and R3 of the State Machine circuit.

AUD 1-2
The Audio 1 and Audio 2 signals are game output game output signals that are generated by custom audio chips B3 and C0 in the Option Switch Input and Audio Output circuit. AUD 1 is the inverse of AUD 2. These signals are applied to the Audio/Regulator 9C2 and 9C2s and ultimately drive speakers 1 and 2.

AVG0-AVG13
Address bits on Vector-Generator Address Bus Lines AVG0-AVG13 are software-generated by Vector Address Controller K9. Bits on lines AVG0-DB2 are ORed together. Bits on lines AVG0-DB2 to pin 2 of R9, producing the BANK SEL signal. BANK SEL is exclusive-Orred with the address bit A10 to produce input address bit A10 for Random-Access Memory N/P1.

BLANK
Black is an active high-level signal generated by counter M3 in the Z-Intensity and Blanking circuit and ORed with Z BLANK by gate 69. When HIGH, BLANK turns off transistors Q6, Q8, and Q10, which kills the RED, GREEN, and BLUE output signals to the display.

BLUE
Blue is a game PCB output signal developed from the data on line DB2. When the data bit on DB2 is HIGH and latch R9 of the Coin Door and Control Panel Output circuit latch the data bit on DB2 to pin 9 of R9. From here, the signal is current amplified and inverted by Q2 and applied to the Right and Left Lockout coils of the game Coin Door.

DD0-7
Microprocessor Data Bus lines DD0-DD7 form a bi-directional data bus between the Microprocessor, the Read-Only Memory, and the Option Switch Input circuits.

DB0-DB8
Microprocessor Data Bus lines DB0-DB8 form a buffered bi-directional data bus between microprocessor data bus buffer F2 and Vector Memory Data Buffer R6. Coin Door and Control Panel Input control buffers L8, M8, and N8. High-Score table latches K2 and J2 and High-Score Table buffer H2.

DIS DAT
Disable Data is an active low-level signal generated by test equipment connected to the DIS DAT test point. DIS DAT is ANDed with the ROM signal by gate E3 to produce the enable signal for the coin Selector input. When enabled DIS DAT passes data from the selected Read-Only Memory to the Microprocessor Data Bus.

DSB
Display Reset is an active low-level signal software-generated by gate L6 of the Halt Circuit. When either RESET or VOST is low, DSB is intended to reset the display. When low, DSB clears State Machine latch P4, DAC Reference and Bipolar Current Sources latch B8, RGB Output latch K10, Vector Scaling latch D7, Z Intensity and Blank latch E6 and counter M3. In addition, DSB1 resets the HALT signal from latch L6 to the high level.

DVS0-DV7
Data on Vector-Generator Data Bus lines DVS0-DV7 are software-generated by the selected Vector Read-Only Memory or Random-Access Memory Memory. If Vector Memory Data Buffer R8 is enabled (BUFFEN is low) and the RGBW line is low, the data lines on lines DVS0-DV7 is passed through R6 to the Buffered Microprocessor Data Bus to be read by the microprocessor. Otherwise, the data on DVS0-DV7 is sent to the Vector Data Switchers and to the Op Code and Intensity Latches.

DVX0-DVX12, DVX13
Data lines on Vector-Generator Data Bus lines DVX0-DVX12 and DVX13 are software-generated by Vector Data Switchers A8, B8, C8, and D8 latch 6 of the Op Code and Intensity Latches. DVX0-DVX7 and DVX12 are the input signals to digital-to-analog converter latch D9. If DVX7 is high, latch D9 operates only in its upper 512 positions for a positive direction of change on the display.

In addition, DVX11 and DVX12 are exclusive-Ored by gate B6 of the Normalization Flag circuit.

DVDY/DY2, DY7
Data bits on Y-Axis Vector Data Lines DVDY/DY2 and DY7 are software-generated by Vector Data Switchers F11, H1, J1, and latch 66 of the Op Code and Intensity Latches circuit. DY5/DY7 and DVX7 are the input signals for digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit. The data carried on these lines represents the Z-axis change from the current location of the display beam. If DVDY7 is low, DAC F9 operates only in its lower 512 positions, which means a negative direction of change on the display. If DV7 is high, DAC F9 operates only in its upper 512 positions for a positive direction of change on the display.

In addition, DVDY0 is applied to latch E8 of the DAC Reference and Bipolar Current Sources circuit. These signals, together with VCTR and VCTR, set the X REF and Y REF voltage levels (via DAC D6).

In addition, DVDY0/DV7 carry data representing the eight different color signals for latch K10 of the RGB Output circuit.

Lines DVDY0/DV7 carry data representing the XIntensity signals for latch E6 of the Z-Intensity and Blanking circuit.

Data on DY0/DY7 are applied to latch D7 of the Vector Scaling circuit. The data carried on these lines represents the number (in binary) that the Vector Scaling circuit uses to divide into the vector drawing time. The vector drawing time n is divided by 2, n equals the number represented by DY5/DV7/Y0.

In addition, DY0/DV7 are exclusive-Ored by gate B6 of the Normalization Flag circuit.

EAROM
The Electrically- alterable ROM Control signal is an active low-level signal software-generated by Address Decoder R3 at address 8000. EAROM is the clock signal for latch K2 in the High-Score Table circuit. EAROMM allows K2 to pass data bits on lines DB3-DB6R to the control lines of EAROM M2.

EAROMM
The Electrically- alterable ROM Read Enable is an active low-level signal software-generated by Address Decoder R2 at address 7700. EAROM is the clock signal for latches J2 and P2 in the High-Score Table circuit. EAROMM allows address bits on lines DB0-AB5 and data bits on lines DB7-DB0 to pass to the address and data input pins of EAROM M2.

Black Widow PCB Signal Name Descriptions

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SP-234 Sheet 8B
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INVERT Y
Invert Y is an active high-level signal developed from the data bit line G6. When clocked by LATCH, latch R6 of the Coin Door and Control Panel Output circuit latches DB0 to pin 9 of R8. WRITE generates a 1010 and WRITE INV closes switch E0 through inverter K9 in the Y-Axis Output circuit. This inverts the Y-axis vector instruction to the display.

INPUT Y
The Input/Output signal is an active low-level signal generated by Address Decoders R2 during addresses 8000 through 8FFF. The Y-axis is selected with YRAM by latch K6 to produce the direction signal for bi-directional data bus buffer N. The Y-axis data bus buffer N is used to pass data to the display.

HALT
The active high-level HALT flag is software-generated by latch L5 of the Halt Flag circuit. Halt is selected with latch K6 of the System CMOS circuit to produce a 7 address input to bit latch R4 of the System RAM.

INTACK
Interrupt Acknowledge is an active low-level signal generated from Address Decoders R2 during addresses 8000 through 8FFF, which is acknowledged from Microprocessor C2 that a interrupt request has been received. INTACK resets counter J4.

INVERT X
Invert X is an active high-level signal developed from the data bit line G6. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches DB0 to bit 8 of R8, latch R6 of the Y-Axis Output circuit, and this inverts the X-axis vector instruction to the display.

LATCH
Latches 3 and 4 are active low-level signal decoder-generated by decoder H7 of the State Machine circuit. LATCH is applied through inverters F7 to the 50 input pins of shift registers A0 to C8 in the Vector Data Shifters circuit. LATCH causes the data bits on lines DVG0-DVG3 to be latched by X8 and 8 lines DVGX3-DVGX7 when X8 is clocked by the 12 MHz clock signal.

LATCH 2
Latch 2 is an active low-level signal decoder-generated by decoder H7 of the State Machine circuit. LATCH 2 is applied through inverters F7 to the 50 input pins of shift register B6 in the Vector Data Shifters circuit. LATCH 2 causes the data bits on lines DVG0-DVG3 to be latched by DB8 to lines DVGX3-DVGX7 when X8 is clocked by the 12 MHz clock signal.

LATCH 3
Latch 3 is an active low-level signal decoder-generated by decoder H7 of the State Machine circuit. LATCH 3 is applied through inverters F7 to the 50 input pins of shift register B8 in the Vector Data Shifters circuit. LATCH 3 causes the data bits on lines DVG0-DVG3 to be latched by X8 to lines DVGX3-DVGX7 when X8 is clocked by the 12 MHz clock signal.

LATCH 4
LATCH 4 is also the clock signal for Op Code and Intensity Latch 6. When LATCH 4 goes low, the data bits on lines DVG0-DVG3 are latched by X8 to lines DVGX3-DVGX7 when X8 is clocked by the 12 MHz clock signal.

LATCH 5
LATCH 5 is also the clock signal for Op Code and Intensity Latch 6. When LATCH 5 goes low, the data bits on lines DVG0-DVG3 are latched by X8 to lines DVGX3-DVGX7 when X8 is clocked by the 12 MHz clock signal.

OP1
The Op Code 1 signal is software-generated by latch 06 in the Op Code and Intensity Latches circuit. When the data line on DVG0 is high, OP1 is set high when D6 is clocked by LATCH. OP1 is multiplexed with a static N6 in the State Machine circuit to produce the A5 address output for State Machine ROM N4. In addition, OP1 is the signal for Vector Address Controller J6. In the Vector Timer circuit, OP1 is gated by K5 and E3 to enable a 110 to be loaded into the D input pin of Vector Timer P6 (if NORM is False, the output of the Timer circuit is disabled).

OP2
The Complementary Op Code 1 signal is software-generated by latch 06 in the Op Code and Intensity Latches circuit. This signal is also used in the Timer circuit as a signal for Vector Address Controller N6 and N8. When OP2 goes low, the count from N6 and N8 is stopped, causing a lowered count from the Vector Timer circuit. This low count is used to draw short vectors on the display. OP2 is also gated with the outputs of the Vector timers by gates L3 and H3 to set STOP to the low level.

OP3
The Op Code 2 signal is software-generated by latch 06 in the Op Code and Intensity Latches circuit. When the data line on DVG0 is high, OP3 is set high when D6 is clocked by LATCH. OP3 is multiplexed with a static N6 in the State Machine circuit to produce the A6 address output for State Machine ROM N4. In addition, OP3 is also gated with the outputs of the Vector timers by gates L3 and H3 to set STOP to the low level.

OP4
The Complementary Op Code 2 signal is software-generated by latch 06 in the Op Code and Intensity Latches circuit. This signal is opposite in state to OP2. If OP2 and OP3 are low, the Vector Data Shifters circuit is enabled. When OP4 goes high, the vector is clocked by the 12 MHz clock signal.
PLAYER 1 LED
The Player 1 LED On signal is developed from the data bit on line DB4. When clocked by CATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on line DB4 to pin 19 of R9. This signal is applied through R10 to light the Player 1 LED on the game Control Panel.

PLAYER 2 LED
The Player 2 LED On signal is developed from the data bit on line DB5. When clocked by CATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB5 to pin 16 of R9. This signal is applied through R10 to light the Player 2 LED on the game Control Panel.

PORT
The active-high level Power-On Reset signal is hardware-generated at pin 4 of F7 in the Power-On Reset circuit. PORT is the power-on signal that starts the count of 0x4 of the Clock circuit.

PORT
The active-low level Power-On Reset signal is hardware-generated at pin 6 of inverter F7 in the Power-On Reset circuit. PORT is grounded when the voltage at pin 3 of R8 is less than about 7 volts or when the RESET test point is shorted to ground. PORT is developed into the reset signal to protect Microprocessor C2.

RAM
The Random-Access Memory Enable is an active-low level signal generated by Address Decoder R2 during addresses 0000 through 0FFF. RAM is the chip-selectable signal for Random-Access Memory NP1. When low, RAM allows data to be read from or written to NP1, depending upon the state of WRITE.

RED
Red is a game PCB output signal developed from the data bit on line D2Y2 in the R-6 Output Circuit. When D2Y2 is high and latch K12 is clocked by D2, the data bit on D2Y2 is inverted and latched to pin 3 of K12. If both BLANK and Z BLANK are low, this data bit is again inverted by gate J10 to turn on Q6. Transistor Q6 generates the RED signal for the display.

RESET
Reset is an active-low level signal generated at pin 6 of K3 from either the Watchdog circuit or the Power-On Reset circuit. The Power-On Reset circuit sets RESET to an active-low level either when the REST test point is shorted to ground or during the time that the power-supply voltages are recovering to their regulated levels. This ensures that the Microprocessor Address Bus is stabilized before the microprocessor begins operation.

The Watchdog circuit sets RESET to an active low level whenever the microprocessor fails to output address 0000 before Watchdog counter H4 has reached its maximum count. RESET is also the clear signal for latch R9 in the Coin Door and Control Panel Output circuit.

In addition, RESET is gated with TGRET by gate L6 in the Halt Flag circuit to produce DISPT.

ROM
The Read-Only Memory Enable is an active-high level signal generated from Address Decoder R2 during addresses 0000 through 0FFF. ROM is output by gate R4 to enable bidirectional data bus buffer F2 to pass data.

In addition, ROM is ANDed with DISPT to enable data buffer E2.

SA
The active-high level Signature Analysis Flag is hardware-generated at pin 12 of inverter J3 when test point SA at pin 13 is grounded. SA is used to place the game PCB in the mode to generate signatures for reading by a Signature Analyzer or the ATARI CAT Box.

SACLK
Signature Analysis Clock is a test point at pin 8 of gate B7 in the State Machine Clock Logic circuit. SACLK is used to apply the clock signal from the Signature Analyzer or ATARI CAT Box for the reading of game PCB signatures.

SAEN
Signature Enable is a test point at pin 8 of gate M5 in the Vector Binary Logic circuit. SAEN is generated by gating VBIEN with the data bit on line AM10 by gates J3 and M5. SAEN is used to enable a Signature Analyzer for the ATARI CAT Box for the reading of game PCB signatures.

SCALE
Scale is an active-high level signal generated by gate B7 of the Vector Scaling circuit. When Q9 is high and counter C7 is counting down, SCALE is set high. SCALE is OFFed with NORM by gate K5 of the Vector Timer circuit to produce the load signal for Vector Timers M6, N6, and N6. When SCALE is high, the Vector Timers perform a load operation for each count of C7 at a 12-Hz rate. This results in a vector drawing time divided by a factor of 2^n where n equals the total counts of C7. When C7 reaches its minimum count, SCALE is set low.

SCALE is gated with VCTR, CNTN, D1V111-D1Y12, and D1V11- D11V12 of the Normalization Flag circuit to produce the clear signal for latch A6.

SALED
Scale Load is an active-low level signal generated by gates N5, L6, and L6 of the Vector Generator circuit. When SCALE is low and N5 and N6 and L6 are all low, SALED is set high.

SALED is the clock signal for Vector Scaling latch D7. When SCALE is high, the data on lines D1V10-D1Y10 are latched to the output pins of D7.

SNP1
Switch Input 1 is an active-low level signal generated by Address Decoder R2 at address 0000 FBP. SNP1 is the direction signal for bidirectional data buffer MB of the Coin Door and Control Panel Input circuit and determines the direction of data flow through buffer MB.

SNP2
Switch Input 2 is an active-low level signal generated by Address Decoder R2 at address 0000 FBP. SNP2 is the direction signal for bidirectional data buffer MB of the Coin Door and Control Panel Input circuit and determines the direction of data flow through buffer MB.

STATCLK
State Clock is an active-low level signal generated by gates N5, L3, and J8 of the Vector Generator circuit. When STROBE, OBP, and D1Y12 are all low, STATCLK is set low. STATCLK is the clock signal for the Coin Door latch K6 in the R-6 Output circuit and latch 8 in the 2.7-kHz Ring and Blankcircuit. When STATCLK goes high, the data bits on D1V1Y12 and D1V1 are latched by K10, and those on D1Y1YV12 are latched by E8.

STOP
Stop is an active-low level signal generated by gate K3 of the Vector Timer circuit. STOP is set low when Vector Timers N6, M6, P6, and R6 have reached their maximum count. If STOP is low, VCTR from Vector Flag latch ES and CNTN from Center Flag latch ES are latched low when ES is clocked by the 12-Hz clock signal.

STROBE
Strobe 0 is an active-low level signal generated by State Machine decoder H7. STROBE is the clock signal for NormaIization Flag latch A6. It is also the STROBE input for Vector Address Controller J9.

STROBE
Strobe 1 is an active-low level signal generated by State Machine decoder H7. If OBP is low, when STROBE goes low, the data latch at the outputs of D7 in the Scaling circuit are loaded into counter C7. When STROBE goes high, C7 begins counting down.

STROBE is the STROBE input for Vector Address Controller J9.

STROBE
Strobe 2 is an active-low level signal generated by State Machine decoder H7. If OBP and D1Y12 are both low, latched C7 from gate J7 is clocked by STROBE. STROBE goes high if OBP and D1Y12 are both low. STROBE is set low when STROBE goes low.

STROBE is the STROBE input for Vector Address Controller J9.

STROBE
Strobe 3 is an active-low level signal generated by State Machine decoder H7. STROBE is the clock signal for Halt Flag latch J8 and is the STROBE input for Vector Address Controller J9.

STROBE
If OBP, OP2, OBP, and VGCK are all low, VCTR from Vector Flag latch J8 and CNTN from Center Flag latch ES are both set high when STROBE goes low.

STO-52
State signals STO-52 are active-high level signals that are high from 5 cycles by State Machine ROM NA. These signals, together with STS are decoded by K7 of the State Machine circuit to produce CATCH/LATCH and STROBE. STS is used to develop STS and is also the STS input for Vector Address Controller J9.

Black Widow PCB Signal Name Descriptions

Black Widow PCB Signal Name Descriptions, cont.
Black Widow PCB Signal Name Descriptions, cont.

ST3
State signal ST3 is an active high-level signal hardware-generated by Decoder Decoder latch A1. ST3 is opposite in state to VGGC, and is delayed by one pulse of the 12.5 MHz clock signal if the Q4 output from State Machine ROM H4 is low and VRIEND is high. If the Q4 output from H4 is high, ST3 is high. When ST3 is high, State Machine decoder H7 is disabled. When ST3 is low, H7 decodes the data on lines STO-ST7 to produce LATCH/LATCH8 and STROBE6/STROBE8.

VCAT, VCTR
The Vector Flag signals are software-generated by Vector Flag latch E5. If OMK, OP9, STROBE6, and VGGC are low and PIRT high, VCAT is set high and VCTR is set low when E5 is locked by the 12.5 MHz clock signal. VCTR is cleared with CNTR by gate M6 to set GO high.

SCALE, CNTR, DVY11-DVY12, and DVX11-DVX12 are gated with VCTR to produce the clear signal for Normalization Flag latch A6. In the Z-Intensity and Blanking circuit, VCTR is the clock signal for latch A6 and the serial input signal for shift register M3.

VCTR and VCAT are used by the DAC Reference and Bipolar Current Sources circuit to set the X BIP, Y BIP, X REF, and Y REF data.

VGGC
The Vector Generator clock signal is generated at pin 18 of buffer B1 in the Microprocessor circuit. VGGC is derived from the 1.5 MHz clock signal and is applied to AND gate J5 of the State Machine Clock Logic circuit. VGGC is the basic timing signal of the State Machine circuit.

VGGD
The Vector Generator Go signal is an active low-level signal software-generated by Address Decoder P3 at address 8860. VGGD is the clear signal for latch LS of the Hall Timer circuit. When low, VGGD sets HALT to the inactive low level.

VRES
Vector Generator Reset is an active low-level signal software-generated by Address Decoder P3 at address 8800. VRES is cleared with RESET by gate L8 of the Hall Timer circuit to produce DISRST.

VMEM
The Vector Memory Select Enable is an active low-level signal software-generated by Address Decoder J7 at address 2000 through 5FFF. VMEM is the select-enable signal for Address Selector latches K8, L8, M8, and N8. When low, VMEM allows the Vector Address Selectors to produce VV, VBUFF, and the AM0-AM12 multiplexed address bits. VMEM is also applied to gate K5 of the State Machine Clock Logic circuit where it is used to generate ST3.

VRAK
The Vector Random-Access Memory Chip Enable is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 2000-27FF. When low, VRAK enables Vector Random-Access Memory K7 to be addressed to either receive or transmit data, depending upon the state of VVR. VRAK is also used to produce the SAEN signal from M8 of the Vector Address Selector circuit.

VROM0
Vector Read-Only Memory Chip Select 0 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 2600-27FF. VROM0 is the chip-select signal for ROM L7 of the Vector Read-Only Memory circuit. When low, VROM0 allows ROM L7 to be addressed and to pass data to the Vector Generator Data Bus.

VROM1
Vector Read-Only Memory Chip Select 1 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 3000-3FFF. VROM1 is the chip-select signal for ROM M7 of the Vector Read-Only Memory circuit. When low, VROM1 allows ROM M7 to be addressed and to pass data to the Vector Generator Data Bus.

VROM2
Vector Read-Only Memory Chip Select 2 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 4000-4FFF. VROM2 is the chip-select signal for ROM N7 of the Vector Read-Only Memory circuit. When low, VROM2 allows ROM N7 to be addressed and to pass data to the Vector Generator Data Bus.

VROM3
Vector Read-Only Memory Chip Select 3 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 5000-5FFF. VROM3 is the chip-select signal for ROM P7 of the Vector Read-Only Memory circuit. When low, VROM3 allows ROM P7 to be addressed and to pass data to the Vector Generator Data Bus.

VV
The Vector Write Enable is an active low-level signal software-generated from Vector Address Selector K8, ANDed with B8 by gate J6, and applied as the write-enable signal for Vector Random-Access Memory K7. When low, VV allows data to be written to K7; when high, VV permits data to be read from K7.

WDCLR
Watchdog Clear is an active low-level signal software-generated by Address Decoder P3 at address 8860. WDCLR is cleared with POR by gate E3 to clear the count of Watchdog counter H4.

WDDS
Watchdog Disable is a test point at pin 9 of AND-gate L4 in the watchdog circuit. When WDDS is grounded, RESET is prevented from going to an active low level (except when the RESET test point is grounded).

WRITE
Write Enable is an active low-level signal generated by gate K4 of the Microprocessor circuit. WRITE is used to enable Address Decoder P3 and Random-Access Memory K7. WRITE is also applied to pin 11 of K8 in the Vector Address Selector circuit to develop VVL.

X BIP
The X-Axis Bipolar Current is set by R98 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pin 18 of X-Axis digital-to-analog converter (DAC) A/89 of the X-Axis Output circuit.

X OUT
X Output is a game PCB output signal generated by the X-Axis Output circuit. X OUT carries the horizontal beam deflection signal for the drawing of vectors on the display.

X REF
The X-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of X-Axis digital-to-analog converter (DAC) A/89 of the X-Axis Output circuit.

Y BIP
The Y-Axis Bipolar Current is set by R96 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pin 16 of Y-Axis digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

Y OUT
Y Output is a game PCB output signal generated by the Y-Axis Output circuit. Y OUT carries the vertical beam deflection signal for the drawing of vectors on the display.

Y REF
The Y-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 15 of Y-Axis digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

Z OUT
Z Intensity and Blanking circuit to produce the select signal for latch F8. This select signal causes the latched data from E6 to be applied as the input signals for latch F6.

Z OUT
Z Intensity Output is a game PCB output signal generated by the Z Intensity and Blanking circuit from either DVY11-DVY12 or ZV22. The output signals from latch H6 are summed at the base of G7, Transistors G7 and Q8 buffer Z OUT before it is sent to the game display circuit to control the display Intensity.

3KHZ
The 3 kHz clock signal is generated at pin 6 of Clock counter F4 and is applied through switch input buffer M9 of the Control Panel Input circuit (when SRIP is low). The 3 kHz clock signal is used to generate the 6 Hz data line DB5. This frequency is the time reference for the Microprocessor C2.

12KHZ
The 12 kHz clock signal is generated at pin 4 of Clock counter F4 and is applied to reset A4 of the High-Resolution Table.

3MHZ
The 3 MHz clock signal is generated at pin 2 of Clock counter F4. The 3 MHz signal is ANDed with B1W and B2W by gate K4 to produce WRITE. IT is also applied to AND gate J5 of the State Machine Clock Logic and to shift register M3 of the Z Intensity and Blanking circuit.

6MHZ
The 6 MHz clock signal is generated at pin 3 of Clock counter F4 and is applied to gate J5 of the State Machine Clock Logic circuit.

12MHZ
The 12 MHz clock signal is generated at pin 10 of Inverter F3 in the Clock circuit. This signal clocks the Vector Timer Shifters, the Vector Flag latch, and the Carrier Flag latch.
Adjusting X- and Y-Axis Video Potentiometers

If you replace the main Gravitar PCB or the display, you may have to make the following adjustments:

1. Enter self-test and advance to diagonal crosshatch pattern (Screen 2).
2. Centering Pots: Adjust X CENTER (R189) and Y CENTER (R212) so that the crosshatch pattern is located at the middle of the screen.
3. Size Pots: Adjust XSIZE (R182) and YSIZE (R213) so that the crosshatch pattern exactly covers the whole visible screen.
4. Linearity Pots: Adjust XLIN (R187) and YLIN (R210) so that the diagonal lines are straight. Since the LIN pots change the size of the displayed picture on the screen, you may have to readjust the SIZE pots in order to get the correct adjustment.
5. Bipolar Pots: Advance to the self-test raster pattern (Screen 4). Adjust XBIP (R69) and YBIP (R68) for a 1-inch high horizontal raster in the center of the screen. Be sure the raster ends are square with the sides of the outer rectangle.
Amplifone Main Wiring Diagram

Amplifone High-Voltage PCB

Note: Unless otherwise specified:
1. All resistor values are in ohms.
2. All capacitor values are in μF.

WARNING
Components identified by shading have special characteristics important to safety and must be replaced only with identical parts.

Amplifone
Color X-Y Display Schematic
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